Digital based DAQ are now a well established technique for the readout of both simple and complex experiments. The flexibility and multipurpose capability offered by this approach make it an ideal solution for the researchers needs. CAEN followed this digital revolution since the beginning and can now offer a wide selection of digitizers that can be used with a variety of detectors in different applications.

Waveform Digitizers

Digitizer Families

Waveform Recording

Digital Pulse Processing (DPP)

Tools

Introduction to Waveform Digitizers

CAEN has developed a complete family of digitizers that consists of several models differing in sampling frequency, resolution, number of channels, form factor, memory size and other parameters.

The following table lists all models currently available. In parallel with the hardware development, CAEN has made a big effort in developing algorithms for the Digital Pulse Processing (DPP); the user can install a DPP algorithm on the FPGA of the digitizer (firmware upgrade), run it on-line and implement new acquisition methods that go beyond the simple waveform recording. A digitizer with DPP becomes a new instrument that represents a fully digital replacement of most traditional modules such as Multi and Single-Channel Analyzers, QDCs, TDCs, Discriminators and many others.

Model (1)	Form Factor	N. of ch. (2) Single-Ended	Max. Sampling Frequency (MS/s) (2)	Resolution (bit)	Input Dynamic Range (Vpp) (2)	Bandwidth (MHz) (2)	Memory (MS/ch) (2)	DPP firmware (3)
x720	VME	8	250	12	2	125	1.25 / 10	PSD
	Desktop/NIM	4 / 2						
x724	VME	8	100	14	0.5 / 2.25 / 10	40	0.5 / 4	PHA, DAW
	Desktop/NIM	4 / 2						
x725 NEW	VME	16 / 8	250	14	0.5 - 2	125	0.64 / 5.12	PHA, PSD, ZLEplus COMING SOON
	Desktop/NIM	8						
x730	VME	16 / 8	500	14	0.5 - 2	250	0.64 / 5.12	PHA, PSD, ZLEplus COMING SOON
	Desktop/NIM	8						
x740	VME	64	62.5	12	2 / 10	30	0.19 / 1.5	QDC
	Desktop/NIM	32						
x751	VME	8 - 4	1000 - 2000	10	1	500	1.8 - 3.6 / 14.4 - 28.8	PSD, ZLEplus
	Desktop/NIM	4 - 2						
x761	VME	2	4000	10	1	1000	7.2 / 57.6	n.a.
	Desktop/NIM	1						
SWITCHED CAPACITOR x742	VME	32+2	5000 (4)	12	1	500	0.128 / 1	n.a.
	Desktop/NIM	16+1						
SWITCHED CAPACITOR x743	VME	16	3200 (4)	12	2.5	500	0.007	n.a.
	Desktop/NIM	8						

(1) The x in the model name is V1 for VME, VX1 for VME64X, DT5 for Desktop and N6 for NIM

(2) The indication "size 1/ size 2" denotes different model versions while "size 1 - size 2" denotes different model operating modes

(3) Digital Pulse Processing (DPP) firmware:
- DPP-PHA: Pulse Height analysis (Trapezoidal Filter);
- DPP-PSD: Pulse Shape Discrimination;
- DPP-ZLEplus: Digital Pulse Processing for the Zero Length Encoding (enhanced Zero Suppression algorithm);
- DPP-DAW: Digital Pulse Processing for Dynamic Acquisition Window
- DPP-QDC: Digital Pulse Processing for Charge to Digital Converter

Note: DPP-CI is no longer supported. To perform Charge Integration, please refer to the DPP-PSD.

(4) Sampling frequency of the analog memory (switched capacitor array); A/D conversion takes place at lower speed (thus generating a Dead Time.)

Introduction to Waveform Digitizers

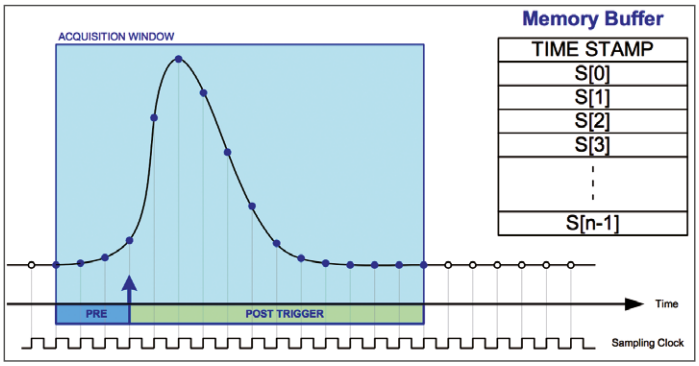
Principle of Operation

CAEN Digitizer shares with a digital oscilloscope essentially the basic operating, where the analogue signal is sampled by a flash ADC, whose output, i.e. the stream of digital samples, is continuously read by an FPGA and stored in a circular memory buffer of a programmable size. At the arrival of the trigger, the buffer is frozen and made available for the readout, while the acquisition can continue in a new buffer.

However, there are few important differences between a digitizer and a commercial digital oscilloscope:

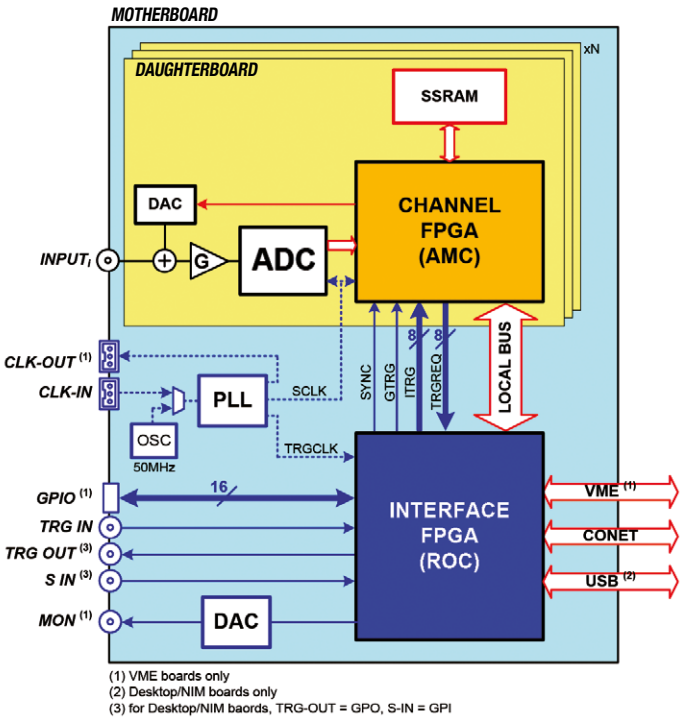
- On-line digital pulse processing (DPP) and data reduction
- Dead-timeless waveform recording
- Independent channel self-triggering and event acquisition
- Multi-board synchronization for system scalability
- High bandwidth data readout links

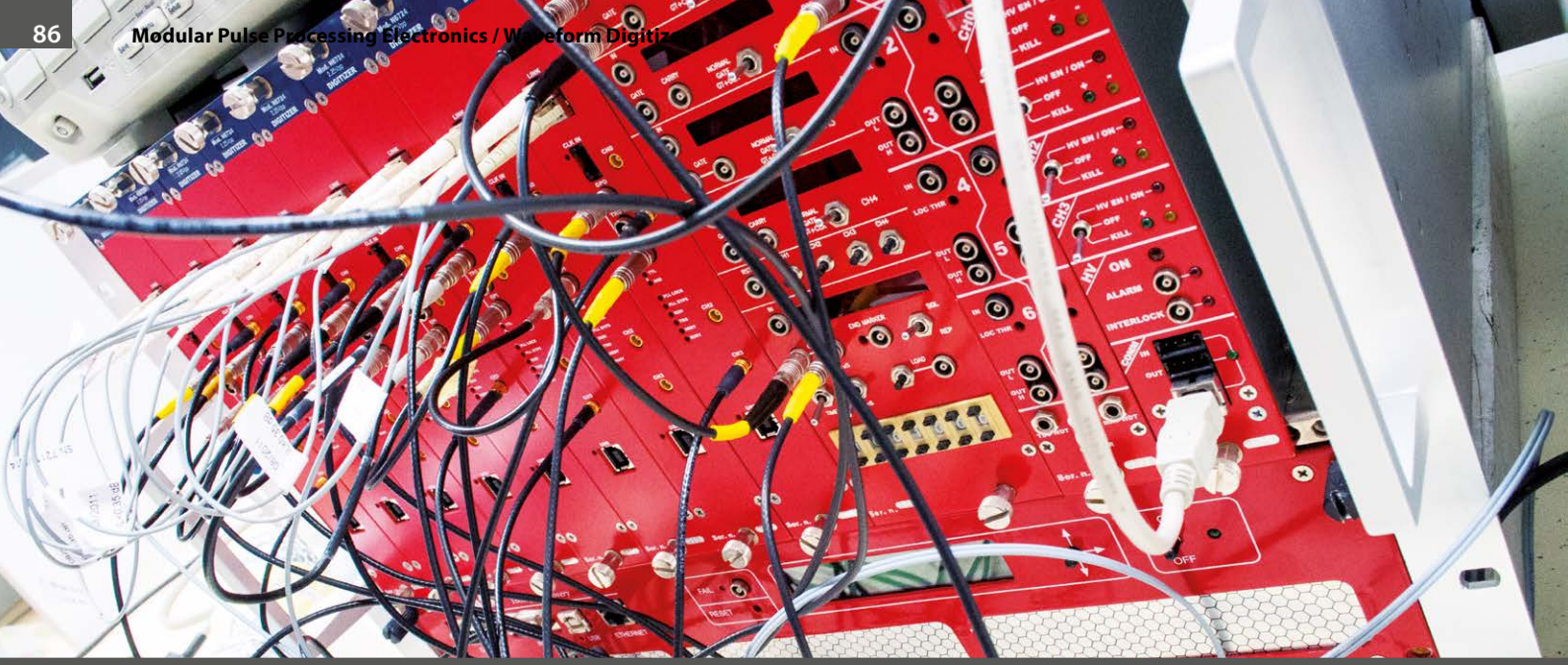
The benefits of the digital approach are great stability and reproducibility, ability to reprogram and tailor the algorithms to the application, ability to preserve the information of the signal along the entire acquisition chain, flexibility, better correction of baseline fluctuation, pile-up, ballistic deficit, etc.. All in one board.



CAEN Digitizer block diagram:

- The motherboard defines the form-factor; it contains one FPGA for the readout interfaces and the services
- The daughterboard defines the type of digitizer; it contains the signal conditioning input stage, the ADCs, the FPGA for the data processing and the memories





Introduction to Waveform Digitizers

1. Digitizers allow for dead-timeless acquisition.

The digitizers have the ability to accept two consecutive triggers very close to each other thanks to the multi-buffer memory management: there is no dead time between an acquisition window and the next one. It is even possible to accept two triggers for which the acquisition windows overlap.

Dead-timeless feature is not supported by all digitizer models and all the firmware.

2. High flexibility of trigger configuration

Each channel of the digitizer is able to implement a digital discriminator that generates a trigger when a certain condition is met; in the basic implementation, this is just a programmable threshold which is continuously compared to the digitized input. More advanced algorithms (digital CFD, timing filters, etc.) are implemented in special DPP firmware. The individual channel self-trigger can be used to generate a global trigger for a simultaneous acquisition of all the channels within a board, can be propagated to the front panel connectors in order to make a multi-board triggering logic or can be used locally for an independent acquisition channel by channel (DPP mode only). It is also possible to combine the individual self-triggers to create a configurable coincidence or anticoincidence logic, either within the board or across multiple digitizers.

3. Scalability and synchronization of multi-board systems

In most cases, the applications that require the use of several channels need to synchronize the acquisition across different digitizers. This is performed according to the following points:

Distribution of a common clock reference in order to have the same sampling clock on all the ADC channels. CAEN digitizers feature a programmable PLL able to generate the sampling clocks locked to an external clock input, whose distribution can be done in parallel from a common source, using a fan-out, as well as through an in-out daisy chain with the ability to use the first board as a clock master (VME models only).

Alignment of the time stamp associated with the triggers to allow off-line reconstruction of the events read from different boards. This can be done by using an external signal as well as through an in-out daisy chain.

Distribution of the triggers from channel to channel and from board to board, according to a certain trigger logic. Each card has different trigger sources: external TRG-IN from the front panel, software trigger and channel self-triggers. All these triggers can be combined in order to make coincidences, majorities, global triggers and other functions.

4. High bandwidth data readout links

The digitizers are designed to provide high rate data transfer to a computer or an external data processing unit. CAEN digitizers have a bandwidth of ≈30MB/s in the case of the USB, about 80MB/s with CONET port up to more than 120MB/s for the VME with 2eSST.

The communication interfaces allow the user to operate post-processing data analysis.

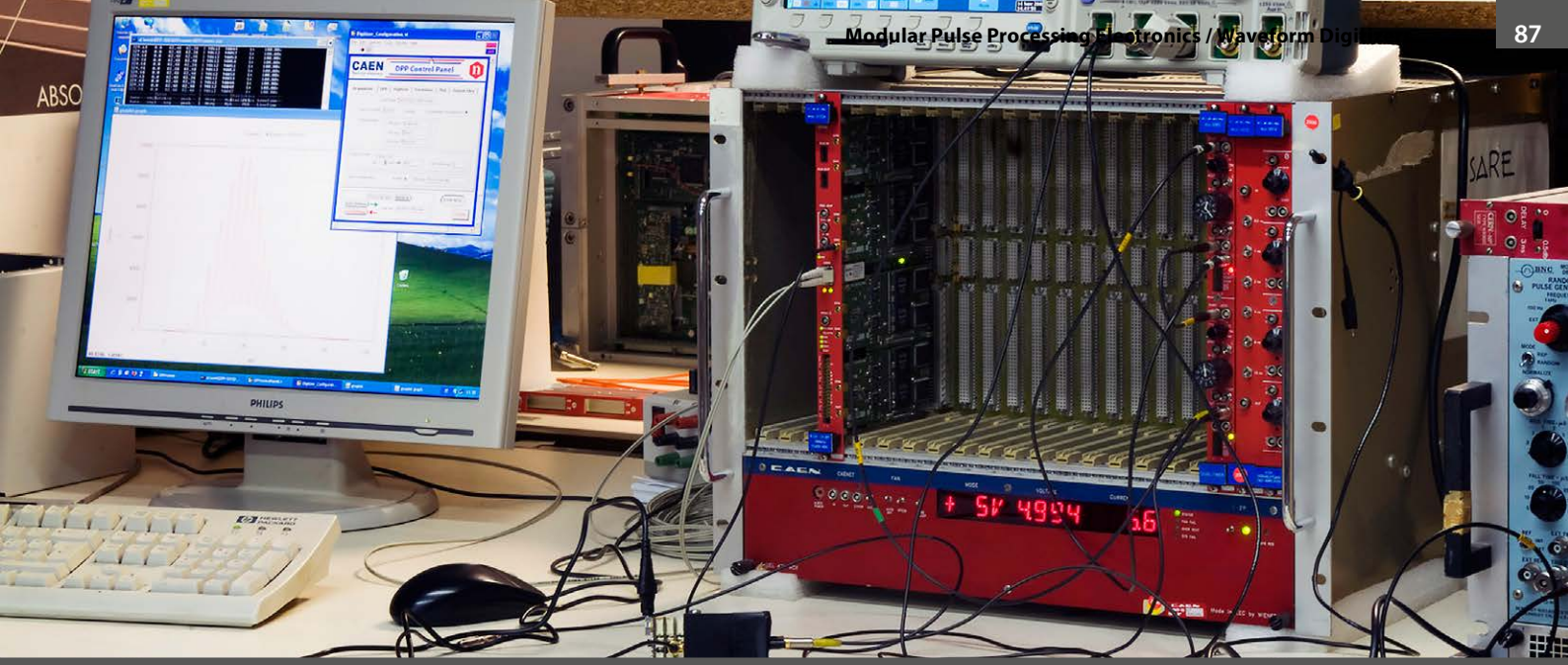
5. Signal Digitization and Pulse Processing

The flash ADC technology has improved significantly in the last decades providing always higher resolution and faster sampling speed. The use of flash ADCs in acquisition boards gives the possibility to convert the analog signal preserving the information required by the experimental activities and the applications of nuclear techniques.

Digital acquisition devices described in this section represent multi-channel waveform digitizers providing time information and digitized signal waveforms through fast communication interfaces, allowing the user to operate post-processing data analysis.

The waveform digitizers integrate also field programmable gate arrays (FPGA) which are able to acquire the information from flash ADC in real time and process it. Algorithms can be programmed, and their parameters can be adjusted to different experimental conditions. Those algorithms may be the digital replacement of the traditional analog signal processing, so that the waveform digitizer embeds different functions in one single board. In particular, it is possible to replace timing filters such as Constant Fraction Discriminators, shaper amplifier, Peak Sensing ADC, QDC, TDC, etc.

Most of the algorithms are implemented at firmware level inside the FPGA, which also manages the overall acquisition and data transfer. Data is read by a software, which is able to both program the digitizer and to perform the acquisition. Most advanced software also provides specific analysis tool, such as peak fitting.



Introduction to Waveform Digitizers

Acquisition Modes

CAEN Digitizers can be operated in different acquisition modes which are introduced in the next sections:

1. Waveform Recording

The digitizer is able to acquire, digitalize and record the input pulse within a programmable time window. Simplified zero suppression functions can be configured. All CAEN digitizers are equipped with their proper default firmware for waveform recording. CAENScope and WaveDump software are available to manage the acquisition. Data can be saved in real time for offline analysis.

Furthermore, the 742 and 743 families, which come with two different switched capacitor chips, are well suitable for high precision time measurement of fast signals. WaveDump and the dedicated WaveCatcher software (free download) can control the acquisition of the two boards respectively.

2. Digital Pulse Processing (DPP)

Where the algorithm inside the FPGA not only acquires the waveform, but also performs additional processing to get a set of significant information like energy, pulse shape and precise timing.

Pulse Height Analysis for gamma ray spectroscopy applies to voltage signals coming from HPGe/Si detectors and Scintillators coupled with Charge Sensitive Preamplifiers.

Works with independent channels event acquisition and in time stamped list mode.

Energy spectra are built by the supported software like the new CoMPASS and MC^{2}Analyzer.

Pulse Shape Discrimination for gated charge integration[(1)] and gamma-neutron discrimination is suited for current signals coming from Scintillators, Gas tubes, SiPM and PMT.

Works with independent channels event acquisition and in energy & timing list mode.

Features digital CFD and timing interpolation for high resolution time information, as well as pulse shape discrimination.

Energy spectra are built by the supported software like the new CoMPASS and the DPP-PSD Control Software.

(1) DPP-CI is no longer supported. To perform Charge Integration, please refer to the DPP-PSD.

Charge to Digital Conversion implements a Gated Integrator receiving signals directly from the detector (no charge preamp required).

Suited for Scintillators and Gas detectors with medium-slow decay time, but can also work with faster detectors such as $LaBr_3$.

Designed for high channel density digitizers, can be used for multi-channel acquisition in Detector Array systems.

Features independent channel acquisition with self-gating capability for the charge integration (no additional delay lines, no external discriminator).

Energy and time stamped list mode provides timing information as well as energy information for spectra calculation.

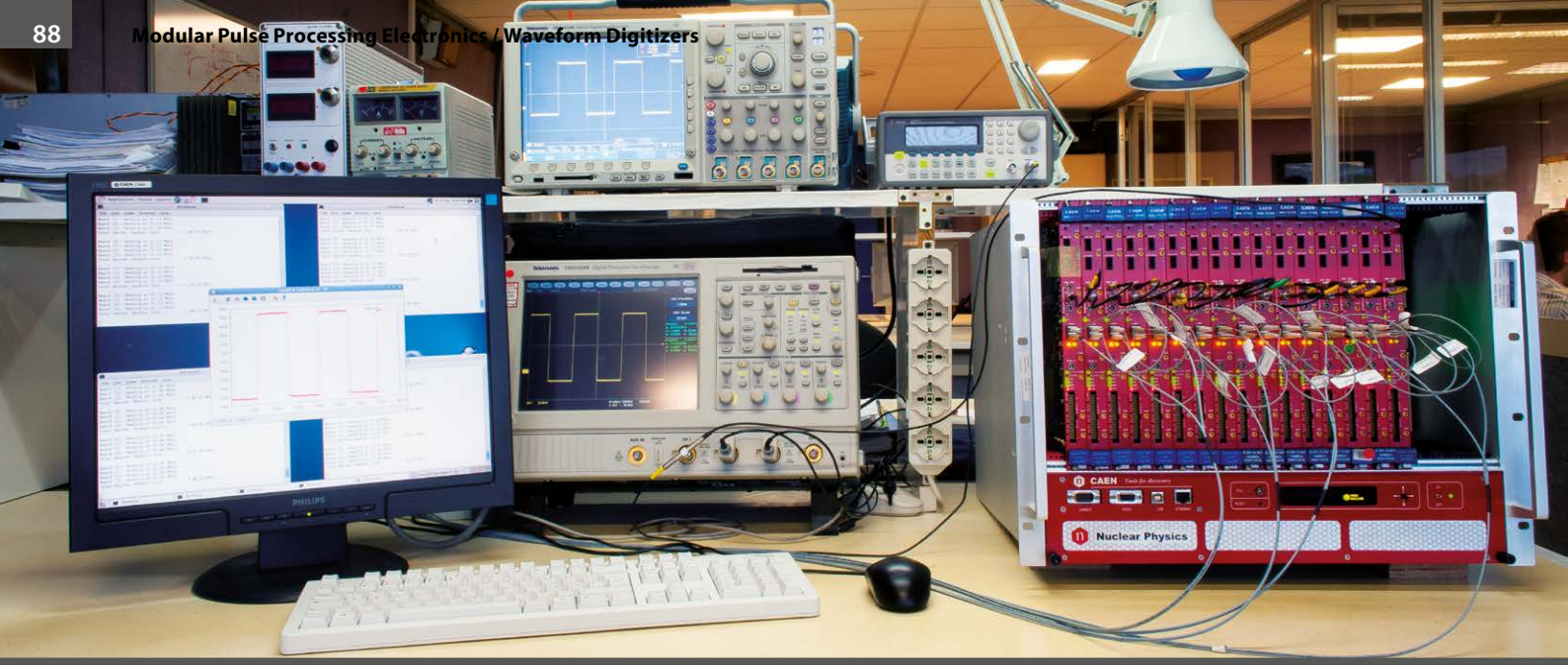
Zero Length Encoding for advanced zero suppression works with a common trigger and simultaneous acquisition on all channels. The digitized waveforms are transferred in compressed mode by suppressing baseline and empty channels.

Dynamic Acquisition Window is suited for zero suppression with trigger-less acquisition systems.

Works in waveform mode and independent channels event acquisition dynamically stretching the acquisition window (record length) to fit the actual input pulse duration.

Software Tools

CAEN provides drivers to integrate its boards in the host PC system, libraries and Demos for software custom development, and configuration software utilities.

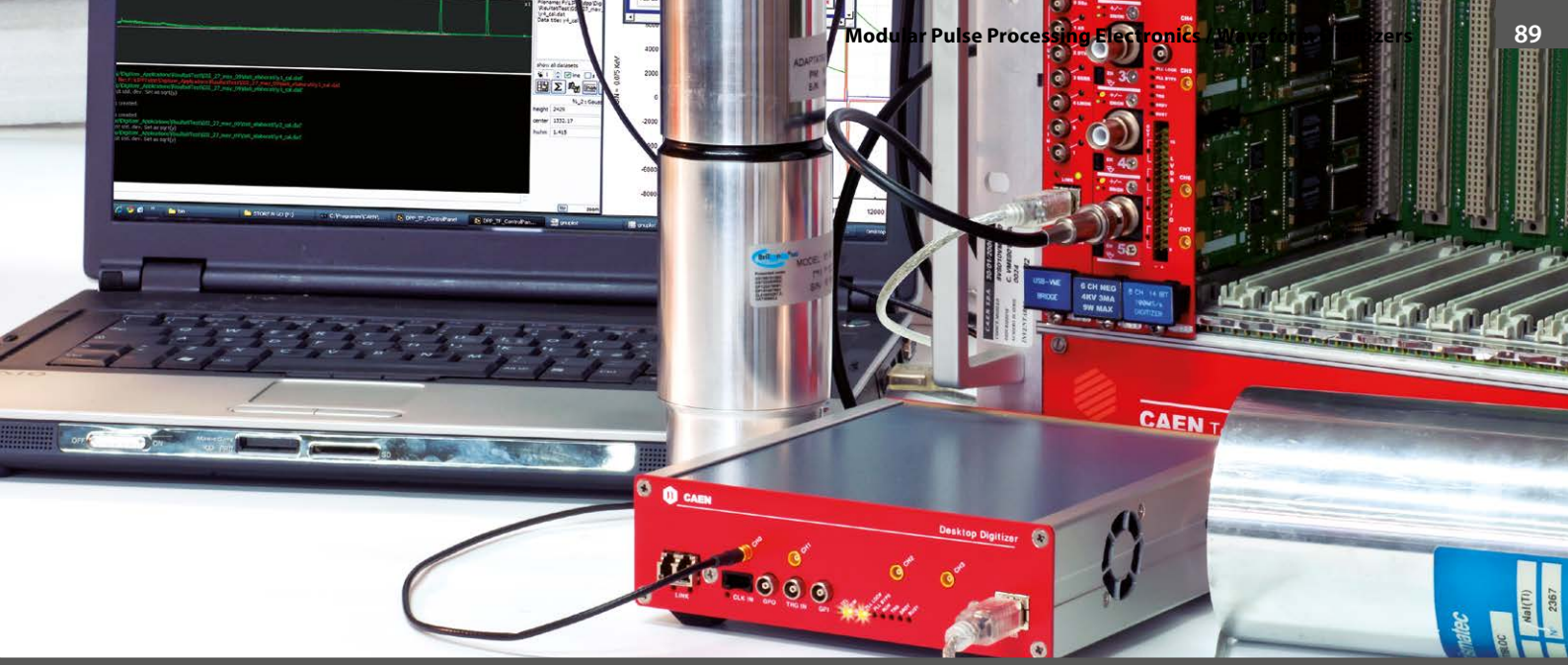


Introduction to Waveform Digitizers

Depending on the final purpose, the user can select the best fitting hardware and firmware solution with the supported CAEN software, as reported in the following table.

Type	Aquisition Mode	Features	Firmware[1]	Software[2]	Family
Digitizer	Digital Pulse Processing	Gated Charge Integration Pulse Shape Discimination	DPP PSD	PSD CAEN CoMPASS CAEN	x720[3]
		Gated Charge Integration Pulse Shape Discrimination Constant Fraction Discriminator & Timing Interpolation	DPP PSD	PSD CAEN CoMPASS CAEN	x725 x730 x751
		Digital QDC Charge Integration	DPP QDC	QDC CAEN CoMPASS CAEN	x740[6]
		Pulse Height Analysis	DPP PHA	MC² CAEN CoMPASS CAEN	x724[4] x725 x730
		Digital Waveform Recorder with Enhanced Zero Surpression	DPP ZLE PLUS	ZLE+ CAEN	x725[5] x730[5] x751
		Digital Waveform Recorder with Zero Suppression for trigger-less acquisition systems	DPP DAW	DAW CAEN	x724
	Waveform Recording	Digital Waveform Recorder	WAVEFORM RECORDING	WAVE DUMP CAEN	x742 x761
				WAVE DUMP CAEN SCOPE CAEN	x720 x724 x725 x730 x740 x751
		Digital Waveform Recorder Charge Integration Constant Fraction Discrimination	WAVEFORM RECORDING	CAEN WAVECATCHER	x743

(1) DPP firmware: free trial version
Waveform Recording firmware (Default): free download
(2) Free Download
(3) DPP-CI firmware and DPP-CI Control Software are no longer supported. To perform Charge Integration please refer to the DPP-PSD firmware and software
(4) DPP-PHA, starting from rev. 128.64 of the AMC FPGA firmware, is no longer supported by x724 models equipped with EP1C4 Altera FPGA
(5) DPP-ZLE Plus for x725 and x730 families: Coming Soon
(6) CoMPASS software for DPP-QDC: Coming Soon
DPP-QDC firmware runs only on x740D digitizer models



Introduction to Waveform Digitizers

Application Notes

CAEN provides a wide selection of application notes, white papers and scientific articles focused on digitizers and their use in different fields. In these documents, the capability and flexibility of CAEN digitizers are well exploited showing their physics-driven development.

Here follows a brief selection:

AN2086 Synchronization of CAEN Digitizers in Multiple Board Acquisition Systems

AN2503 Charge Integration: Analog Vs. Digital

AN2506 Digital Gamma Neutron discrimination with Liquid Scintillators

AN2508 CAEN Digital Pulse Height Analyser a digital approach to Radiation Spectroscopy

AN2770 Digital ToF Measurements of Fast Neutrons in a Spallation Neutron Source

WP2081 Digital Pulse Processing in Nuclear Physics

AR2614 Tests of PMT Signal Read-out in a Liquid Argon Dark Matter Detector with a New Fast Waveform Digitizer

AR2613 Special nuclear material detection with a mobile multi-detector system

AR2612 First demonstration of a Compton gamma imager based on silicon photomultipliers

AR2593 Diamond detectors for fast neutron measurements at pulsed spallation sources

GD2827 How to make coincidences with CAEN digitizers

AN3250 Pulse Shape Discrimination with different CAEN digitizers running DPP-PSD firmware

AN3251 Time Measurements with CAEN Waveform Digitizers

All these documents are available for download in the Document Library section of CAEN website.

APPLICATIONS

- Nuclear and Particle Physics
- Dark Matter and Astroparticle Physics
- Fast Neutron spectroscopy, Fusion Plasma diagnostics
- Environmental monitoring, Homeland Security

FORM FACTOR

VME64 VME64X NIM DESKTOP

FEATURES

USB Digital I/O Optical Link

A cost- effective, general purpose choice

720 Digitizer Family

8/4/2 Ch. 12-bit 250 MS/s Digitizer

Overview

The 720 is a family of 12-bit and 250 MS/s Flash ADC Waveform Digitizers with 2 Vpp of input dynamic range and DC offset adjustment.

It is available in three form factors: VME (8 input channels), NIM (4 or 2 input channels) and Desktop (4 or 2 input channels).

Considering the sampling frequency and the bit number, these digitizers are well suited for mid-fast signals as the ones coming from liquid or inorganic scintillators coupled to PMTs or Silicon Photomultipliers.

The acquisition capabilities take advantage of the multi-buffer organization of the channel memory (divisible into a maximum of 1024 buffers). The data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer. Two memory sizes are available according to the different versions of the x720 model: 1.25 MS/ch or 10 MS/ch.

The on-board FPGAs can run default firmware for waveform recording (including 'Zero suppression' and 'data reduction' methods that allow substantial savings in data amount readout and processing) as well as Digital Pulse Processing algorithms (DPP) making the digitizer an enhanced system for Physics applications. In addition to the existing firmware selection, CAEN is willing to collaborate with customers for developing custom solutions.

A common acquisition trigger signal can be provided externally, via front panel digital input connector, or via software. Alternatively, each channel can generate a trigger request when the input pulse goes under/over a programmable threshold; the trigger requests can be used either locally by the channel (independent triggering with DPP firmware) or processed by the board to generate a common trigger causing all the enable channels to acquire an event simultaneously (default firmware). The trigger from one board can be provided out on a front panel digital output connector.

720 family supports multi-board synchronization making a multi-board system where all ADCs result to be synchronized to a common clock source, and ensuring Trigger Time Tag alignment. Once synchronized, all data will be aligned and coherent across multiple x720 boards.

Firmware	Software	Features
WAVEFORM RECORDING	WAVE DUMP CAEN, SCOPE CAEN	Digital Waveform Recording
DPP PSD	PSD CAEN, CoMPASS CAEN	Charge Integration Pulse Shape Discrimination

Features

- 12-bit @ 250 MS/s
- Analog inputs on MCX coax. connectors (single ended)
- VME64/VME64X (8 ch.), NIM (4 or 2 ch.) and Desktop (4 or 2 ch.) modules
- 2 Vpp input dynamic range with programmable DC offset adjustment
- Algorithms for Digital Pulse Processing (DPP)
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, Control Software for default and DPP firmware, C and LabVIEW libraries

Technical Specifications

GENERAL

Form Factor
1-unit wide, 6U VME64/VME64X

1-unit wide NIM

154x50x164 mm³ (WxHxD) Desktop

ANALOG INPUT

Channels
8 channels, single ended (VME)

4/2 channels, single ended (NIM, Desktop)

Impedance
50 Ω

Connector
MCX

Full Scale Range (FSR)
2 Vpp

Bandwidth
125 MHz

Offset
Programmable DAC for DC offset adjustment. Range: ±1 V

DIGITAL CONVERSION

Resolution
12 bits

Sampling rate
31.25 to 250 MS/s simultaneously on each channel

ADC CLOCK GENERATION

Clock source: internal/external

On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference

MEMORY

1.25 MS/ch or 10 MS/ch Multi Event Buffer with independent read and write access divisible into 1 ÷ 1024 buffers

Programmable event size and pre-post trigger

TRIGGER

Trigger sources
Self-trigger: channel over/under threshold for either Common or Individual (DPP firmware only) trigger generation

External-trigger: Common by TRG-IN or Individual by LVDS connectors (DPP firmware only)

Software-trigger: Common by software command

Trigger propagation
TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp
Default firmware: 31-bit counter, 16 ns resolution, 17 s range(*); 48-bit extension by firmware

DPP-CI/PSD Firmware: 32-bit counter, 4 ns resolution, 17 s range; 64-bit extension by software

SYNCHRONIZATION

Clock propagation
Daisy chain (VME only) by CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization
Sync Start/Stop by digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed

An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/100 MHz DAC FPGA controlled output with four operating modes: Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTERFACE

Optical Link
CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM and Desktop direct, VME via V1718 bridge)
USB 2.0 compliant

Transfer rate up to 30 MB/s

VME
VME 64X compliant

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.5 A @ 12 V (Typ.)

NIM: 2.9 A @ +6 V, 90 mA @ -6 V

VME: 4 A @ +5 V, 200 mA @ +12 V, 200 mA @ -12 V

(*) Trigger Logic and Trigger Time Stamp counter operate at 125 MHz (i.e. 8 ns or 1/2 ADC clock cycles), while the counter value is read at a frequency of 62.5 MHz (i.e. 16 ns).

Ordering Options

Code	Description	Form Factor
WDT5720BXAAA	DT5720B - 4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	Desktop
WDT5720CXAAA	DT5720C - 2 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	Desktop
WDT5720DXAAA	DT5720D - 4 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	Desktop
WDT5720EXAAA	DT5720E - 2 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	Desktop
WN6720BXAAAA	N6720B - 4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	NIM
WN6720CXAAAA	N6720C - 2 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	NIM
WN6720DXAAAA	N6720D - 4 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	NIM
WN6720EXAAAA	N6720E - 2 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	NIM
WV1720EXAAAA	V1720E - 8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	6U-VME64
WV1720GXAAAA	V1720G - 8 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE	6U-VME64
WVX1720EXAAA	VX1720E - 8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE	6U-VME64X
WVX1720GXAAA	VX1720G - 8 Ch. 12 bit 250 MS/s Digitizer: 10MS /ch, C20, SE	6U-VME64X
WFWDPPNGAA20	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x720)	ALL

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

APPLICATIONS

- **Nuclear and Particle Physics**
- **X-ray and Gamma Spectroscopy with HPGe, Silicon detectors**
- **Spectroscopic Imaging for Homeland Security**
- **Segmented detectors, Medical Imaging, Material science**

FORM FACTOR

VME64 VME64X NIM DESKTOP

FEATURES

USB Digital I/O Optical Link

Ideal for high resolution detectors

724 Digitizer Family

8/4/2 Ch. 14-bit 100 MS/s Digitizer

Overview

The 724 is a family of 14-bit and 100 MS/s Flash ADC Waveform Digitizers with 2.25 Vpp of input dynamics (optionally 0.5 or 10 Vpp) and DC offset adjustment.

It is available in three form factors: VME (8 input channels), NIM (4 or 2 input channels) and Desktop (4 or 2 input channels).

Considering the sampling frequency and the bit number, these digitizers are well suited for high resolution detectors as Silicon, HPGe coupled to Charge Sensitive Preamplifiers or inorganic scintillators like NaI or CsI.

The acquisition capabilities take advantage of the multi-buffer organization of the channel memory (divisible into a maximum of 1024 buffers). The data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer. Two memory sizes are available according to the different versions of the x724 model: 512 kS/ch or 4 MS/ch.

The on-board FPGAs can run default firmware for waveform recording (including 'Zero suppression' and 'data reduction' methods that allow substantial savings in data amount readout and processing) as well as Digital Pulse Processing algorithms (DPP) making the digitizer an enhanced system for Physics applications. In addition to the existing firmware selection, CAEN is willing to collaborate with customers for developing custom solutions.

A common acquisition trigger signal can be provided externally, via front panel digital input connector, or via software. Alternatively, each channel can generate a trigger request when the input pulse goes under/over a programmable threshold; the trigger requests can be used either locally by the channel (independent triggering with DPP firmware) or processed by the board to generate a common trigger causing all the enable channels to acquire an event simultaneously (default firmware). The trigger from one board can be provided on a front panel digital output connector.

724 family supports multi-board synchronization making a multi-board system where all ADCs result to be synchronized to a common clock source, and ensuring Trigger Time Tag alignment. Once synchronized, all data will be aligned and coherent across multiple x724 boards.

Firmware	Software	Features
WAVEFORM RECORDING	WAVE DUMP CAEN, SCOPE CAEN	Digital Waveform Recording
DPP PHA	MC² CAEN, CoMPASS CAEN	Pulse Height Analysis
DPP DAW	DAW CAEN	Digital Waveform Recording with Zero Suppression for trigger-less acquisition systems

Features

- 14-bit @ 100 MS/s
- Analog inputs on MCX coax. connectors (single ended)
- VME64/VME64X (8 ch.), NIM (4 or 2 ch.) and Desktop (4 or 2 ch.) modules
- 0.5, 2.25 or 10 Vpp input dynamic range with programmable DC offset adjustment
- Algorithms for Digital Pulse Processing (DPP)
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, Control Software for default and DPP firmware, C and LabVIEW libraries

Technical Specifications

GENERAL

Form Factor

1-unit wide, 6U VME64/VME64X

1-unit wide NIM

154x50x164 mm^3 (WxHxD) Desktop

ANALOG INPUT

Channels

8 channels, single ended (VME)

4/2 channels, single ended (NIM, Desktop)

Impedance

50 Ω (2.25 and 0.5 Vpp), 1 k Ω (10 Vpp)

Connector

MCX

Full Scale Range (FSR)

2.25 Vpp (0.5 or 10 Vpp by ordering code)

Bandwidth

40 MHz

Offset

Programmable DAC for DC offset adjustment. Range: ±1.125 @ 2.25 Vpp, ±0.25 @ 0.5 Vpp, ±5 V @ 10 Vpp

DIGITAL CONVERSION

Resolution

14 bits

Sampling rate

32.2 to 100 MS/s simultaneously on each channel

ADC CLOCK GENERATION

Clock source: internal/external

On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference

MEMORY

512 KS/ch or 4 MS/ch Multi-Event Buffer with independent read and write access divisible into 1 ÷ 1024 buffers. Programmable event size and pre-post trigger

TRIGGER

Trigger sources

Self-trigger: channel over/under threshold for either Common or Individual (DPP firmware only) trigger generation

External-trigger: Common by TRG-IN or Individual by LVDS connectors (DPP firmware only)

Software-trigger: Common by software command

Trigger propagation

TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp

Default firmware: 31-bit counter, 20 ns resolution, 21 s range(*); 48-bit extension by firmware

DPP-PHA Firmware: 30-bit counter, 10 ns resolution, 10 s range; 64-bit extension by software

DPP-DAW Firmware: 31-bit counter, 10 ns resolution, 21 s range; 64-bit extension by software

SYNCHRONIZATION

Clock propagation

Daisy chain (VME only) through CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization

Acquisition Synchronization

Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed

An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/100 MHz DAC FPGA controlled output with four operating modes: Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTERFACE

Optical Link

CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM and Desktop direct, VME via V1718 bridge)

USB 2.0 compliant

Transfer rate up to 30 MB/s

VME

VME 64X compliant

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.7 A @ 12 V (Typ.)

NIM: 3.9 A @ +6 V, 90 mA @ -6 V

VME: 4.5 A @ +5 V, 200 mA @ +12 V, 200 mA @ -12 V

(*) Trigger Logic and Trigger Time Stamp counter operate at 100 MHz (i.e. 10 ns or 1 ADC clock cycle), while the counter value is read at a frequency of 50 MHz (i.e. 20 ns).

Ordering Options

Code	Description	Form Factor
WDT5724BXAAA	DT5724B - 4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE	Desktop
WDT5724CXAAA	DT5724C - 2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE	Desktop
WDT5724FXAAA	DT5724F - 4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE	Desktop
WDT5724GXAAA	DT5724G - 2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE	Desktop
WN6724BXAAAA	N6724B - 4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch,C20, SE	NIM
WN6724CXAAAA	N6724C - 2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE	NIM
WN6724FXAAAA	N6724F - 4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch,C20, SE	NIM
WN6724GXAAAA	N6724G - 2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE	NIM
WV1724EXAAAA	V1724E - 8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE	6U-VME64
WV1724GXAAAA	V1724G - 8 Ch. 14 bit 100 MS/s Digitizer: 512KS/ch, C20, SE	6U-VME64
WVX1724EXAAA	VX1724E - 8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE	6U-VME64X
WPERS0172401	724 Customization - 10Vpp Input Range, SE	ALL
WPERS0172402	724 Customization - 500mVpp Input Range, SE	ALL
WFWDPPTFAAAA	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (x724)	ALL
WFWDPPDAWXEA	DPP-DAW - Digital Pulse Processing with Dynamic Acquisition Window (x724)	ALL

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

APPLICATIONS

- Nuclear and Particle Physics
- Dark Matter and Astroparticle Physics
- Fast Neutron spectroscopy
- Homeland Security

FORM FACTOR

VME64 VME64X NIM DESKTOP

FEATURES

USB Digital I/O Optical Link

Maximum flexibility

NEW 725 Digitizer Family

16/8 Ch. 14-bit 250 MS/s Digitizer

Overview

The 725 is a family of 14-bit and 250 MS/s Flash ADC Waveform Digitizers with software selectable 0.5 Vpp or 2 Vpp (default) input dynamic range and DC offset adjustment.

It is available in three form factors: VME (16/8 input channels), NIM (8 input channels) and Desktop (8 input channels).

Considering the sampling frequency and the bit number, these digitizers are well suited for mid-fast signals as the ones coming from liquid or inorganic scintillators coupled to PMTs or Silicon Photomultipliers, and others.

The acquisition capabilities take advantage of the multi-buffer organization of the channel memory (divisible into a maximum of 1024 buffers). The data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer. Two memory sizes are available according to the different versions of the x725 model: 640 kS/ch or 5.12 MS/ch.

The on-board FPGAs can run default firmware for waveform recording as well as Digital Pulse Processing algorithms (DPP) making the digitizer an enhanced system for Physics applications. In addition to the existing firmware selection, CAEN is willing to collaborate with customers for developing custom solutions.

A common acquisition trigger signal can be provided externally, via front panel digital input connector, or via software. Alternatively, each channel can generate a trigger request when the input pulse goes under/over a programmable threshold; the trigger requests can be used either locally by the channel (independent triggering with DPP firmware) or processed by the board to generate a common trigger causing all the enable channels to acquire an event simultaneously (default firmware). The trigger from one board can be provided on a front panel digital output connector.

725 family supports multi-board synchronization making a multi-board system where all ADCs result to be synchronized to a common clock source, and ensuring Trigger Time Tag alignment. Once synchronized, all data will be aligned and coherent across multiple x725 boards.

Firmware	Software	Features
WAVEFORM RECORDING	WAVE DUMP CAEN, SCOPE CAEN	Digital Waveform Recording
DPP PSD	PSD CAEN, CoMPASS CAEN	Charge Integration Pulse Shape Discrimination Constant Fraction Discriminator
DPP PHA	MC² CAEN, CoMPASS CAEN	Pulse Height Analysis
DPP ZLE PLUS	ZLE CAEN	Digital Waveform Recording with Enhanced Zero Suppression **Coming soon**

Features

- 14-bit @ 250 MS/s
- Analog inputs on MCX coax. connectors
- VME64/VME64X (16/8 ch.), NIM (8 ch.) and Desktop (8 ch.) modules
- 0.5 and 2 Vpp input dynamic range with programmable DC offset adjustment
- Algorithms for Digital Pulse Processing (DPP)
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, Control Software for default and DPP firmware, C and LabVIEW libraries

Technical Specifications

GENERAL

Form Factor

1-unit wide, 6U VME64/VME64X

1-unit wide NIM

154x50x164 mm³ (WxHxD) Desktop

ANALOG INPUT

Channels

16/8 channels, single ended (VME)

8 channels, single ended (NIM, Desktop)

Impedance

50 Ω

Connector

MCX

Full Scale Range (FSR)

0.5 or 2 Vpp (default) software selectable

Bandwidth

125 MHz

Offset

Programmable DAC for DC offset adjustment. Range: ±1 V @ 2 Vpp, ±0.25 V @ 0.5 Vpp

DIGITAL CONVERSION

Resolution

14 bits

Sampling rate

250 MS/s simultaneously on each channel

ADC CLOCK GENERATION

Clock source: internal/external

On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference

MEMORY

640 kS/ch or 5.12 MS/ch Multi-Event Buffer with independent read and write access divisible into 1 ÷ 1024 buffers. Programmable event size and pre-post trigger

TRIGGER

Trigger source

Self-trigger: channel over/under threshold for either Common or Individual (DPP firmware only) trigger generation

External-trigger: Common by TRG-IN or Individual by LVDS connectors (DPP firmware only)

Software-trigger: Common by software command

Trigger propagation

TRG-OUT (VME) / GPO (NIM, Desktop) digital output

Trigger Time Stamp

Default Firmware: 31-bit counter, 16 ns resolution, 17 s range(*); 48-bit extension by firmware

DPP-PHA/PSD: 31-bit counter, 4 ns resolution, 8 s range; 47-bit extension by firmware; 10-bit and 4 ps fine time stamp by digital CFD; 64-bit extension by software

SYNCHRONIZATION

Clock propagation

Daisy chain (VME only) through CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization

Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory Full, Individual Trg-Out and other functions can be programmed

An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/100 MHz DAC FPGA controlled output with four operating modes:

Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTERFACE

Optical Link

CAEN CONET proprietary protocol,

up to 80 MB/s transfer rate

Daisy chainable: it is possible to

connect up to 8/32 ADC modules to a

single Optical Link Controller (Mod.A2818/A3818)

VME

VME 64X compliant

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: TBD

NIM: TBD

VME:	V1725	V1725x
	5.2 A @ +5 V	TBD
	750 mA @ +12 V	
	-12 V not used	

Ordering Options

Code	Description	Form Factor
WDT5725XAAAA	DT5725 - 8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE	Desktop
WDT5725BXAAA	DT5725B - 8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE	Desktop
WN6725XAAAAA	N6725 - 8 Ch. 12/14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE	NIM
WN6725BXAAAA	N6725B - 8 Ch. 12/14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE	NIM
WV1725XAAAAA	V1725 - 16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE	6U-VME64
WV1725BXAAAA	V1725B - 16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE	6U-VME64
WV1725CXAAAA	V1725C - 8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE	6U-VME64
WV1725DXAAAA	V1725D - 8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE	6U-VME64
WVX1725XAAAA	VX1725 - 16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE	6U-VME64X
WVX1725BXAAA	VX1725B - 16 Ch. 14 bit 250 MS/s Digitizer: 5.12MSch, CE30, SE	6U-VME64X
WVX1725CXAAA	VX1725C - 8 Ch. 14 bit 250 MS/s Digitizer: 640kS/c, CE30, SE	6U-VME64X
WVX1725DXAAA	VX1725D - 8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE	6U-VME64X
WFWDPPTFAA25	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (x725)	ALL
WFWDPPNGAA25	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x725)	ALL

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

(*) Trigger Logic and Trigger Time Stamp counter operate at 125 MHz (i.e. 8 ns or 2 ADC clock cycles), while the counter value is read at a frequency of 62.5 MHz (i.e. 16 ns).

APPLICATIONS

- Nuclear and Particle Physics
- Dark Matter and Astroparticle Physics
- Fast Neutron spectroscopy
- Homeland Security

FORM FACTOR

VME64 VME64X NIM DESKTOP

FEATURES

USB Digital I/O Optical Link

Excellent resolution and fast sampling combined

730 Digitizer Family

16/8 Ch. 14-bit 500 MS/s Digitizer

Overview

The 730 is a family of 14-bit and 500 MS/s Flash ADC Waveform Digitizers with software selectable 0.5 Vpp or 2 Vpp (default) input dynamic range and DC offset adjustment.

It is available in three form factors: VME (16/8 input channels), NIM (8 input channels) and Desktop (8 input channels).

Considering the sampling frequency and the bit number, these digitizers are well suited for mid-fast signals as the ones coming from liquid or inorganic scintillators coupled to PMTs or Silicon Photomultipliers, and others.

The acquisition capabilities take advantage of the multi-buffer organization of the channel memory (divisible into a maximum of 1024 buffers). The data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer. Two memory sizes are available according to the different versions of the x730 model: 640 kS/ch or 5.12 MS/ch.

The on-board FPGAs can run default firmware for waveform recording as well as Digital Pulse Processing algorithms (DPP) making the digitizer an enhanced system for Physics applications. In addition to the existing firmware selection, CAEN is willing to collaborate with customers for developing custom solutions.

A common acquisition trigger signal can be provided externally, via front panel digital input connector, or via software. Alternatively, each channel can generate a trigger request when the input pulse goes under/over a programmable threshold; the trigger requests can be used either locally by the channel (independent triggering with DPP firmware) or processed by the board to generate a common trigger causing all the enable channels to acquire an event simultaneously (default firmware). The trigger from one board can be provided out on a front panel digital output connector.

730 family supports multi-board synchronization making a multi-board system where all ADCs result to be synchronized to a common clock source, and ensuring Trigger Time Tag alignment. Once synchronized, all data will be aligned and coherent across multiple x730 boards.

Firmware	Software	Features
WAVEFORM RECORDING	WAVE DUMP CAEN, SCOPE CAEN	Digital Waveform Recording
DPP PSD	PSD CAEN, CoMPASS CAEN	Charge Integration Pulse Shape Discrimination Constant Fraction Discriminator
DPP PHA	MC² CAEN, CoMPASS CAEN	Pulse Height Analysis
DPP ZLE PLUS	ZLE CAEN	Digital Waveform Recording with Enhanced Zero Suppression **Coming soon**

Features

- 14-bit @ 500 MS/s
- Analog inputs on MCX coax. connectors
- VME64/VME64X (16/8 ch.), NIM (8 ch.) and Desktop (8 ch.) modules
- 0.5 and 2 Vpp input dynamic range with programmable DC offset adjustment
- Algorithms for Digital Pulse Processing (DPP)
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, Control Software for default and DPP firmware, C and LabVIEW libraries

Technical Specifications

GENERAL

Form Factor

1-unit wide, 6U VME64/VME64X

1-unit wide NIM

154x50x164 mm³ (WxHxD) Desktop

ANALOG INPUT

Channels

16/8 channels, single ended (VME)

8 channels, single ended (NIM, Desktop)

Impedance

50 Ω

Connector

MCX

Full Scale Range (FSR)

0.5 or 2 Vpp (default) software selectable

Bandwidth

250 MHz

Offset

Programmable DAC for DC offset adjustment. Range: ±1 V @ 2 Vpp, ±0.25 V @ 0.5 Vpp

DIGITAL CONVERSION

Resolution

14 bits

Sampling rate

500 MS/s simultaneously on each channel

ADC CLOCK GENERATION

Clock source: internal/external

On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference

MEMORY

640 kS/ch or 5.12 MS/ch Multi-Event Buffer with independent read and write access divisible into 1 ÷ 1024 buffers. Programmable event size and pre-post trigger

TRIGGER

Trigger source

Self-trigger: channel over/under threshold for either Common or Individual (DPP firmware only) trigger generation

External-trigger: Common by TRG-IN or Individual by LVDS connectors (DPP firmware only)

Software-trigger: Common by software command

Trigger propagation

TRG-OUT (VME) / GPO (NIM, Desktop) digital output

Trigger Time Stamp

Default Firmware: 31-bit counter, 16 ns resolution, 17 s range(*); 48-bit extension by firmware

DPP-PHA/PSD: 31-bit counter, 2 ns resolution, 4 s range; 47-bit extension by firmware; 10-bit and 2 ps fine time stamp by digital CFD; 64-bit extension by software

SYNCHRONIZATION

Clock propagation

Daisy chain (VME only) through CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization

Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed

An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/100 MHz DAC FPGA controlled output with four operating modes: Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTERFACE

Optical Link

CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM and Desktop direct, VME via V1718 bridge)

USB 2.0 compliant

Transfer rate up to 30 MB/s

VME

VME 64X compliant

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 2.8 A @ 12 V (Typ.)

NIM: 4.9 @ +6 V, 250 mA @ -6 V

VME: V1730	V1730B	V1730x
8.2 A @ +5 V	10.2 A @ +5 V	TBD
840 mA @ +12 V	840 mA @ +12 V	
-12 V not used	-12 V not used	

Ordering Options

Code	Description	Form Factor
WDT5730XAAAA	DT5730 - 8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE	Desktop
WDT5730BXAAA	DT5730B - 8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE	Desktop
WN6730XAAAAA	N6730 - 8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE	NIM
WN6730BXAAAA	N6730B - 8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE	NIM
WV1730XAAAAA	V1730 - 16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE	6U-VME64
WV1730BXAAAA	V1730B - 16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE	6U-VME64
WV1730CXAAAA	V1730C - 8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE	6U-VME64
WV1730DXAAAA	V1730D - 8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE	6U-VME64
WVX1730XAAAA	VX1730 - 16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE	6U-VME64X
WVX1730BXAAA	VX1730B - 16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE	6U-VME64X
WVX1730CXAAA	VX1730C - 8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE	6U-VME64X
WVX1730DXAAA	VX1730D - 8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE	6U-VME64X
WFWDPPTFAA30	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (x730)	ALL
WFWDPPNGAA30	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x730)	ALL

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

(*) Trigger Logic and Trigger Time Stamp counter operate at 125 MHz (i.e. 8 ns or 4 ADC clock cycles), while the counter value is read at a frequency of 62.5 MHz (i.e. 16 ns).

APPLICATIONS

- Nuclear and Particle Physics
- Neutrino Physics
- Spectroscopic Imaging
- Homeland Security

FORM FACTOR

VME64 VME64X NIM DESKTOP

FEATURES

USB Digital I/O Optical Link

Very high channel density

740 Digitizer Family

64/32 Ch. 12-bit 62.5 MS/s Digitizer

Overview

The 740 is a family of 12-bit and 62.5 MS/s Flash ADC Waveform Digitizers with 2 Vpp (optionally 10 Vpp) of input dynamic range and DC offset adjustment. It is available in three form factors: VME (64 input channels), NIM (32 input channels) and Desktop (32 input channels). Such a high channel density, thanks to an octal ADC chip, implies that most channel settings are common to groups of 8 channels (one group per ADC chip).

Considering the sampling frequency and the bit number, these digititizers are well suited for mid-slow signals as the ones coming from inorganic scintillators coupled to PMTs, gaseous detectors and others. Sampling rate can be reduced thanks to the firmware decimation option.

The acquisition capabilities take advantage of the multi-buffer organization of the channel memory (divisible into a maximum of 1024 buffers). The data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer. Two memory sizes are available according to the different versions of the x740 model: 192 kS/ch or 1.5 MS/ch.

The On-board FPGAs can run default firmware for waveform recording as well as Digital Pulse Processing algorithms (DPP) making the digitizer an enhanced system for Physics application. Special DPP-QDC firmware is supported by x740D digitizer models. In addition to the existing firmware selection, CAEN is willing to collaborate with customers for developing custom solutions.

A common acquisition trigger signal can be provided externally, via front panel digital input connector, or via software. Alternatively, in the default firmware, each 8-channel group can generate a trigger request when at least one of the channels goes under/over a programmable threshold; the requests from the groups are processed by the board to generate a common trigger causing all the channels to acquire an event simultaneously. In the DPP firmware each channel can trigger the event acquisition independently on the others upon the pulse under/over threshold. The trigger from one board can be provided on a front panel digital output connector.

740 family supports multi-board synchronization making a multi-board system where all ADCs result to be synchronized to a common clock source, and ensuring Trigger Time Tag alignment. Once synchronized, all data will be aligned and coherent across multiple x740 boards.

(1) DPP-QDC firmware runs only on x740D digitizer models

Firmware	Software	Features
WAVEFORM RECORDING	WAVE DUMP CAEN, SCOPE CAEN	Digital Waveform Recording
DPP QDC	QDC CAEN, CoMPASS CAEN	Digital QDC Charge Integration (1)

Features

- 12-bit @ 62.5 MS/s
- Analog inputs on ERNI SMC connectors
- VME64/VME64X (64 ch.), NIM (32 ch.) and Desktop (32 ch.) modules
- 2 or 10 Vpp input dynamic range with programmable DC offset adj.
- Sampling rate decimation factor (software selectable)
- Algorithms for Digital Pulse Processing (DPP)
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, Control Software for default and DPP firmware, C and LabVIEW libraries

Technical Specifications

GENERAL

Form Factor

1-unit wide, 6U VME64/VME64X

1-unit wide NIM

154x50x164 mm^3 (WxHxD) Desktop

ANALOG INPUT

Channels

64 channels, single ended (VME); 32 channels, single endend (NIM)

32 channels, single endend (Desktop) or 16 channels by auxiliary on-board connectors

Impedance

50 Ω (2 Vpp), 1 k Ω (10 Vpp)

Connector

ERNI SMC Dual Row 68pin (VME, NIM and Desktop)

MCX auxiliary (Desktop)

Full Scale Range (FSR)

2 or 10 Vpp (by ordering code)

Bandwidth

30 MHz

Offset

Programmable DAC for DC offset adjustment per each 8-channel group

Range: ±1 V @ 2 Vpp, ±5 V @ 10 Vpp

DIGITAL CONVERSION

Resolution

12 bits

Sampling rate

62.5 MS/s simultaneously on each channel (65 MS/s using external clock)

Down to 62.5/128 MS/s by programmable decimation factor ($62.5/2^n$ MS/s; n=0,..,7)

ADC CLOCK GENERATION

Clock source: internal/external

On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference

MEMORY

192 kS/ch or 1.5 MS/ch Multi-Event Buffer with independent read and write access divisible into 1 ÷ 1024 buffers. Programmable event size and pre-post trigger

TRIGGER

Trigger sources

Self-trigger: channel over/under threshold for either Common or Individual (DPP firmware only) trigger generation

External-trigger: Common by TRG-IN or Individual by LVDS connectors (DPP firmware only)

Software-trigger: Common by software command

Trigger propagation

TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp

Default firmware: 31-bit counter, 16 ns resolution, 17 s range(*); 48-bit extension by firmware

DPP-QDC Firmware: 32-bit counter, 16 ns resolution, 68 s range; 48-bit extension by firmware; 64-bit extension by software

SYNCHRONIZATION

Clock propagation

Daisy chain (VME only) through CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization

Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/100 MHz DAC FPGA controlled output with four operating modes: Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTERFACE

Optical Link

CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM and Desktop direct, VME via V1718 bridge)

USB 2.0 compliant

Transfer rate up to 30 MB/s

VME

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.9 A @ 12 V (Typ.)

NIM: 3.9 A @ +6 V, 490 mA @ -6 V

VME: 5.6 A @ +5 V, 250 mA @ +12 V, -12 V not used

(*) Trigger Logic and Trigger Time Stamp counter operate at 125 MHz (i.e. 8 ns or 1/2 ADC clock cycles), while the counter value is read at a frequency of 62.5 MHz (i.e. 16 ns).

Ordering Options

Code	Description	Form Factor
WDT5740XAAAA	DT5740 - 32 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE	Desktop
WDT5740CXAAA	DT5740C - 10Vpp input 32 Ch. 12 bit 62.5MS/s Digitizer: 192kS/ch, EP3C16, SE	Desktop
WDT5740DXAAA	DT5740D - 32 Ch. 12 bit 62.5 MS/s Digitizer: 192kSch, EP3C40, SE	Desktop
WN6740DXAAAA	N6740D - 32 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C40, SE	NIM
WN6740XAAAAA	N6740 - 32 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE	NIM
WN6740CXAAAA	N6740C - 10Vpp input 32 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE	NIM
WV1740XAAAAA	V1740 - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE	6U-VME64
WV1740AXAAAA	V1740A - 10Vpp input 64ch 12bit 62.5MS/s Digitizer: 1.5 MS/ch, EP3C16, SE	6U-VME64
WV1740BXAAAA	V1740B - 64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE	6U-VME64
WV1740CXAAAA	V1740C - 10Vpp input 64ch 12bit 62.5MS/s Digitizer: 192kS/ch, EP3C16, SE	6U-VME64
WV1740DXAAAA	V1740D - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C40, SE	6U-VME64
WVX1740XAAAA	VX1740 - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kS/ch, EP3C16, SE	6U-VME64X
WVX1740AXAAA	VX1740A - 10Vpp input 64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE	6U-VME64X
WVX1740BXAAA	VX1740B - 64 Ch. 12 bit 62.5 MS/s Digitizer: 1.5 MS/ch, EP3C16, SE	6U-VME64X
WVX1740CXAAA	VX1740C - 10Vpp input 64 Ch. 12 bit 62.5 MS/s Digitizer: 192 KS/ch, EP3C16, SE	6U-VME64X
WVX1740DXAAA	VX1740D - 64 Ch. 12 bit 62.5 MS/s Digitizer: 192kSch, EP3C40, SE	6U-VME64X
WFWDPPQDCAAA	DPP-QDC- Digital Pulse Processing for Time Stamped Digital QDC (x740)	ALL

Accessories

A746D
32 Channel Adapter for LEMO connector

A746B
64 Channel Adapter for LEMO connector

A746B
64 Channel Adapter for LEMO connector

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

APPLICATIONS

- **Nuclear and Particle Physics**
- **Dark Matter and Astroparticle Physics**
- **Fast Neutron spectroscopy**
- **Fusion Plasma diagnostic, Homeland Security**

FORM FACTOR

VME64 VME64X NIM DESKTOP

FEATURES

USB Digital I/O Optical Link

Well suited for fast signals

751 Digitizer Family

8-4/4-2 Ch. 10-bit 1/2 GS/s Digitizer

Overview

The 751 is a family of 10-bit and 1 GS/s Flash ADC Waveform Digitizers with 1 Vpp of input dynamic range (optionally 0.2 Vpp) and DC offset adjustment. It can work also at 2 GS/s when operating in Dual Edge Sampling (DES) mode, interleaving pairs of input channels.

It is available in three form factors: VME (8 input channels), NIM and Desktop (4 input channels). When in DES mode, half the number of channels is available.

Considering the sampling frequency and the bit number, These digitizers are well suited for fast signals as the ones coming from fast organic, inorganic and liquid scintillators coupled to PMTs or Silicon Photomultipliers, Diamond detectors and others.

The acquisition capabilities take advantage of the multi-buffer organization of the channel memory (divisible into a maximum of 1024 buffers). The data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer. Two memory sizes are available according to the different versions of the x751 model: 1.8-3.6 MS/ch or 14.4-28.8 MS/ch.

The on-board FPGAs can run default firmware for waveform recording as well as Digital Pulse Processing algorithms (DPP) making the digitizer an enhanced system for Physics applications. In addition to the existing firmware selection, CAEN is willing to collaborate with customers for developing custom solutions.

A common acquisition trigger signal can be provided externally, via front panel digital input connector, or via software. Alternatively, each channel can generate a trigger request when the input pulse goes under/over a programmable threshold; the trigger requests can be used either locally by the channel (independent triggering with DPP firmware) or processed by the board to generate a common trigger causing all the enable channels to acquire an event simultaneously (default firmware). The trigger from one board can be provided out on a front panel digital output connector.

751 family supports multi-board synchronization making a multi-board system where all ADCs result to be synchronized to a common clock source, and ensuring Trigger Time Tag alignment. Once synchronized, all data will be aligned and coherent across multiple x751 boards.

Firmware	Software	Features
WAVEFORM RECORDING	WAVE DUMP CAEN, SCOPE CAEN	Digital Waveform Recording
DPP PSD	PSD CAEN, CoMPASS CAEN	Charge Integration Pulse Shape Discrimination Constant Fraction Discriminator
DPP ZLE PLUS	ZLE CAEN	Digital Waveform Recording with Enhanced Zero Suppression

Features

- 10-bit @ 1-2 GS/s
- Analog inputs on MCX coax. connectors (single ended)
- VME64/VME64X (8-4 ch.), NIM (4-2 ch.) and Desktop (4-2 ch.) modules
- 0.2 or 1 Vpp input dynamic range with programmable DC offset adj.
- Algorithms for Digital Pulse Processing (DPP)
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, Control Software for default and DPP firmware, C and LabVIEW libraries

Technical Specifications

GENERAL

Form Factor
1-unit wide, 6U VME64/VME64X

1-unit wide NIM

154x50x164 mm³ (WxHxD) Desktop

ANALOG INPUT

Channels
8-4 channels, single ended (VME)

4-2 channels, single ended (NIM, Desktop)

Impedance
50 Ω (1 and 0.2 Vpp)

Connector
MCX

Full Scale Range (FSR)
1 Vpp (0.2 Vpp by ordering code)

Bandwidth
500 MHz

Offset
Programmable DAC for DC offset adjustement. Range: ±0.5 V @ 1 Vpp, ±0.1 V @ 0.2 Vpp

DIGITAL CONVERSION

Resolution
10 bits

Sampling rate
250 to 1000 MS/s simultaneously on each channel (double in DES mode)

ADC CLOCK GENERATION

Clock source: internal/external

On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference

MEMORY

1.835 MS/ch (3.6 MS/ch in DES mode) or 14.4 MS/ch (28.8 MS/ch in DES mode) Multi Event Buffer with independent read and write access divisible into 1 ÷ 1024 buffers

Programmable event size and pre-post trigger

TRIGGER

Trigger source
Self-trigger: channel over/under threshold for either Common or Individual (DPP firmware only) trigger generation

External-trigger: Common by TRG-IN or Individual by LVDS connectors (DPP firmware only)

Software-trigger: Common by software command

Trigger propagation
TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp
Default Firmware, DPP-ZLE: 31-bit counter, 16 ns resolution, 17 s range(*); 48-bit extension by firmware

DPP-PSD Firmware: 32-bit counter, 1 ns resolution, 4 s range, expandable to 64-bit; 10-bit and 1 ps fine time stamp by digital CFD; 64-bit extension by software

SYNCHRONIZATION

Clock propagation
Daisy chain (VME only) through CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization
Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/100 MHz DAC FPGA controlled output with four operating modes: Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTERFACE

Optical Link
CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM and Desktop direct, VME via V1718 bridge)
USB 2.0 compliant

Transfer rate up to 30 MB/s

VME
VVME 64X compliant

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.8 A @ 12 V (Typ.)

NIM: 3.9 A @ +6 V, 120 mA @ -6 V

VME: 6.5 A @ +5 V, 200 mA @ +12 V, 300 mA @ -12 V

(*) Trigger Logic and Trigger Time Stamp counter operate at 125 MHz (i.e. 8 ns or 1/2 ADC clock cycles), while the counter value is read at a frequency of 62.5 MHz (i.e. 16 ns).

Ordering Options

Code	Description	Form Factor
WDT5751XAAAA	DT5751 - 2/4 Ch. 10 bit 2/1 GS/s Digitizer: 3.6/1.8MS/ch, EP3C16, SE	Desktop
WN6751XAAAAA	N6751 - 2/4 Ch. 10 bit 2/1 GS/s Digitizer: 3.6/1.8MS/ch, EP3C16, SE	NIM
WN6751CXAAAA	N6751C - 2/4 Ch. 10 bit 2/1 GS/s Digitizer: 28.8/14.4MS/ch, EP3C16, SE	NIM
WV1751XAAAAA	V1751 - 4/8 Ch. 10 bit 2/1 GS/s Digitizer: 3.6/1.8MS/ch, EP3C16, SE	6U-VME64
WV1751CXAAAA	V1751C - 4/8 Ch. 10 bit 2/1 GS/s Digitizer: 28.8/14.4MS/ch, EP3C16, SE	6U-VME64
WVX1751XAAAA	VX1751 - 4/8 Ch. 10 bit 2/1 GS/s Digitizer: 3.6/1.8MS/ch, EP3C16, SE	6U-VME64X
WVX1751CXAAA	VX1751C - 4/8 Ch. 10 bit 2/1 GS/s Digitizer: 28.8/14.4MS/ch, EP3C16, SE	6U-VME64X
WPERS0175102	751 Customization - 200 mVpp Input Range, SE	ALL
WFWDPPNGAA51	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x751)	ALL
WFWDPPZLAA51	DPP-ZLE - Digital Pulse Processing Zero Length Encoding for (x751)	ALL

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

APPLICATIONS

- **High resolution Time of Flight**
- **Optical Physics**
- **Fast Neutron spectroscopy**

FORM FACTOR

VME64 VME64X NIM DESKTOP

FEATURES

USB Digital I/O Optical Link

The fastest Flash ADC of the series

761 Digitizer Family

2/1 Ch. 10-bit 4 GS/s Digitizer

Overview

The 761 is a family of 10-bit and 4 GS/s Flash ADC Waveform Digitizers with 1 Vpp of input dynamic range and DC offset adjustment.

It is available in three form factors: VME (2 input channels), NIM (1 input channel) and Desktop (1 input channel).

Considering the sampling frequency and the bit number, these digitiziers are well suited for very fast signals as the ones coming from PMTs or Silicon Photomultipliers, Diamond detectors and others.

The acquisition capabilities take advantage of the multi-buffer organization of the channel memory (divisible into a maximum of 1024 buffers). The data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer. Two memory sizes are available according to the different versions of the x761 model: 7.2 MS/ch or 57.6 MS/ch.

The on-board FPGAs allow for real-time data processing. In addition to the existing default firmware for waveform recording, CAEN is willing to collaborate with customers for developing custom solutions.

A common acquisition trigger signal can be provided externally, via front panel digital input connector, or via software. Alternatively, each channel can generate a trigger request when the input pulse goes under/over a programmable threshold; the trigger requests are processed by the board to generate a common trigger causing all the enabled channels to acquire an event simultaneously. The trigger from one board can be provided out on a front panel digital output connector.

761 family supports multi-board synchronization making a multi-board system where all ADCs result to be synchronized to a common clock source, and ensuring Trigger Time Tag alignment. Once synchronized, all data will be aligned and coherent across multiple x761 boards.

Features

- 10-bit @ 4 GS/s
- Analog inputs on MCX coax. connectors (single ended)
- VME64/VME64X (2 ch.), NIM (1 ch.) and Desktop (1 ch.) modules
- 1 Vpp input dynamic range with programmable DC offset adj.
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, C and LabVIEW libraries

Firmware	Software	Features
WAVEFORM RECORDING	WAVE DUMP CAEN	Digital Waveform Recording

Technical Specifications

GENERAL

Form Factor
1-unit wide, 6U VME64/VME64X

1-unit wide NIM

154x50x164 mm^3 (WxHxD) Desktop

ANALOG INPUT

Channels
2 channels, single ended (VME)

1 channel, single ended (NIM, Desktop)

Impedance
50 Ω

Connector
MCX

Full Scale Range (FSR)
1 Vpp

Bandwidth
1 GHz

Offset
Programmable DAC for DC offset adjustement. Range: ±0.5 V

DIGITAL CONVERSION

Resolution
10 bits

Sampling rate
4 GS/s simultaneously on each channel

ADC CLOCK GENERATION

Clock source: internal/external

On-Board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference

MEMORY

7.2 MS/ch or 57.6 MS/ch Multi Event Buffer with independent read and write access divisible into 1 ÷ 1024 buffers

Programmable event size and pre-post trigger

TRIGGER

Trigger source
Self-trigger: channel over/under threshold for Common trigger generation

External-trigger: Common by TRG-IN connector

Software-trigger: Common by software command

Trigger propagation
TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp
31-bit counter, 16 ns resolution, 17 s range(*); 48-bit extension by firmware

SYNCHRONIZATION

Clock propagation
Daisy chain (VME only) through CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization
Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

ANALOG MONITOR (VME only)

12-bit/100 MHz DAC FPGA controlled output with four operating modes: Trigger Majority / Test Pulses / Memory Occupancy / Voltage Level

COMMUNICATION INTEFRACE

Optical Link
CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM and Desktop direct, VME via V1718 bridge)
USB 2.0 compliant

Transfer rate up to 30 MB/s

VME
VME 64X compliant

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.8 A @ 12 V (Typ.)

NIM: 3.9 A @ +6 V, 120 mA @ -6 V

VME: 6.5 A @ +5 V, 200 mA @ +12 V, 300 mA @ -12 V

(*) Trigger Logic and Trigger Time Stamp counter operate at 125 MHz (i.e. 8 ns or 32 ADC clock cycles), while the counter value is read at a frequency of 62.5 MHz (i.e. 16 ns).

Ordering Options

Code	Description	Form Factor
WDT5761XAAAA	DT5761 - 1 Ch.10 bit 4 GS/s Digitizer: 7.2MS/ch, EP3C16, SE	Desktop
WN6761XAAAAA	N6761 - 1 Ch. 10 bit 4 GS/s Digitizer: 7.2Ms/ch, EP3C16, SE	NIM
WV1761XAAAAA	V1761 - 2 Ch.10 bit 4 GS/s Digitizer: 7.2MS/ch, EP3C16, SE	6U-VME64
WV1761CXAAAA	V1761C - 2 Ch. 10 bit 4 GS/s Digitizer: 57.6MS/ch, EP3C16, SE	6U-VME64
WVX1761XAAAA	VX1761 - 2 Ch.10 bit 4 GS/s Digitizer: 7.2MS/ch, EP3C16, SE	6U-VME64X
WVX1761CXAAA	VX1761C - 2 Ch. 10 bit 4 GS/s Digitizer: 57.6MS/ch, EP3C16, SE	6U-VME64X

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

APPLICATIONS

- Nuclear and Particle Physics
- Astroparticle Physics
- Time of Flight
- Medical Imaging (PET)

FORM FACTOR

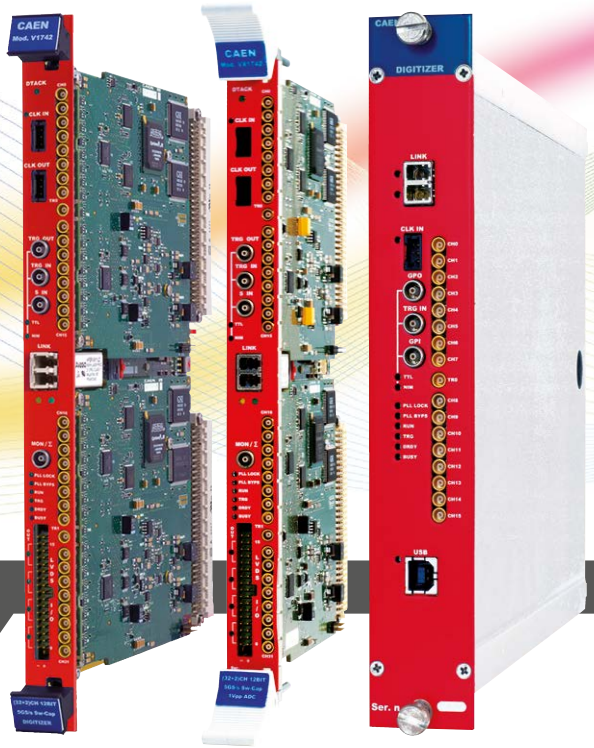
VME64 VME64X NIM DESKTOP

FEATURES

USB Digital I/O Optical Link

Based on the DRS4 a Switched Capacitor Array

Very fast Switched Capacitor Digitizer with high channel density



742 Digitizer Family

32+2/16+1 Ch. 12-bit 5 GS/s Digitizer

Overview

The 742 is a family of 12-bit and 5 GS/s Switched Capacitor Waveform Digitizers with 1 Vpp of input dynamic range and DC offset adjustment, based on the DRS4 chip (Paul Scherrer Institute design).

It is available in three form factors: VME (32+2 input channels), NIM (16+1 input channels) and Desktop (16+1 input channels). Additional analog inputs, each one managing 16 channels (two adjacent 8-channel groups), serve as fast local trigger.

Considering the sampling frequency and the bit number, these digitizers are well suited for very fast signals as the ones coming from fast scintillators coupled to PMTs, Silicon Photomultipliers, APD, Diamond detectors and others.

The analog input signals are continuously sampled inside the DRS4 chip in a circular memory buffer (1024 cells) at the default sampling frequency of 5 GS/s (200 ps of sampling period); 2.5 or 1 GS/s frequencies can also be selected. As a trigger signal arrives, all analog memory buffers are frozen and subsequently digitized with a resolution of 12 bits into a digital memory buffer with independent read and write access. Two memory sizes are available according to the different version of the x742 model: 128 or 1024 events with 1024 samples per event.

During analog to digital conversion process, the x742 cannot handle other triggers, thus generating a Dead Time.

A common acquisition trigger signal can be provided externally via front panel digital input connector or via software, but it can also be generated internally thanks to channel self-trigger capability (only after the A/D conversion, with a trigger latency of 250 ns). The trigger from one board can be provided out on a front panel digital output connector.

Additional analog inputs (TR0 for NIM/Desktop, TR0 and TR1 for VME), can be used as low-latency external trigger signals. These special inputs can be also sampled into the DRS4s analog memory buffers for applications where high resolution timing and time analysis with a common reference signal (like a trigger or system clock) is required.

Firmware	Software	Features
WAVEFORM RECORDING	WAVE DUMP CAEN	Digital Waveform Recording

742 family supports multi-board synchronization making a multi-board system where all ADCs result to be synchronized to a common clock source, and ensuring Trigger Time Tag alignment. Once synchronized, all data will be aligned and coherent across multiple x742 boards.

Features

- 12-bit @ 5 GS/s, 1024 samples per event
- 5, 2.5, 1 GS/s software selectable sampling frequencies
- Analog inputs on MCX coaxial connectors
- VME64/VME64X (32+2 ch.), NIM (16+1 ch.) and Desktop (16+1 ch.) modules
- 1 Vpp input dynamic range with programmable DC offset adj.
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Demo software tools, C and LabVIEW libraries

x742 is based on the DRS4 a Switched Capacitor Array. This technology relies on a set of capacitors that continuously sample the analog input signals. As soon as the trigger is issued, capacitors are decoupled from the input signals with a time interval from each other that is the sampling period.

The trigger therefore freezes the currently stored signal in the sampling capacitance cells. Subsequently the cells are multiplexed into the 12 bit ADC.

Technical Specifications

GENERAL

Form Factor
1-unit wide, 6U VME64/VME64X

1-unit wide NIM

154x50x164 mm^3 (WxHxD) Desktop

ANALOG INPUT

Channels
32+2 channels, single ended (VME)

16+1 channels, single ended (NIM, Desktop)

Impedance
50 Ω

Connector
MCX

Full Scale Range (FSR)
1 Vpp

Bandwidth
500 MHz

Offset
Programmable DAC for DC offset adjustment per channel or 8-channel group. Range: ±1 V

TR0 TR1 Analog Inputs
Special inputs (MCX, 50 Ω) for fast local trigger and high resolution timing reference

NIM/LVTTL signals also supported

DIGITAL CONVERSION

Switched Capacitor array
Domino Ring Sampler chip (DRS4) serving 8+1 channels

1024 storage cells per channel (200 ns minimun recorded time per event)

Resolution
12 bits

Sampling rate
5 (default) - 2.5 - 1 GS/s software selectable, simultaneously on each channel

Dead Time for Event A/D Conversion
110 µs analog inputs only; 181 µs analog inputs + TR0, TR1 inputs

CLOCK GENERATION

Synchronization clock source: internal/external

On-Board PLL provides generation of main board clocks from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference

MEMORY

128 events/ch or 1024 events/ch (1024 samples per event) Multi-Event Buffer

TRIGGER

Trigger source
Self-trigger: channel over/under threshold by digital discriminator on all channels (after A/D conversion; involves a 250-ns latency)

Fast local trigger: by analog discriminator on TR0 and TR1 special inputs (each TRn signal triggers 16 channels)

External-trigger: Common by TRG-IN connector

Software-trigger: Common by software command

Trigger propagation
TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp
30-bit counter, 8.5 ns resolution, 9 s range

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA

Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

SYNCHRONIZATION

Clock propagation
Daisy chain (VME only) through CLK-IN/CLK-OUT connectors

One-to-many clock distribution from an external clock source

Clock Cable delay compensation

Acquisition Synchronization
Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)

External Trigger Time Stamp reset

COMMUNICATION INTEFRACE

Optical Link
CAEN CONET proprietary protocol, up to 80 MB/s transfer rate

Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM & Desktop direct, VME via V1718 bridge)
USB 2.0 compliant

Transfer rate up to 30 MB/s

VME
VME 64X compliant

Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.7 A @ 12 V (Typ.)

NIM: 3.9 A @ +6 V, 90 mA @ -6 V

VME: 5.5 A @ +5 V, 200 mA @ +12 V, 300 mA @ -12 V

Ordering Options

Code	Description	Form Factor
WDT5742XAAAA	DT5742 - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	Desktop
WDT5742BXAAA	DT5742B - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event), EP3C16, SE	Desktop
WN6742XAAAAA	N6742 - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	NIM
WN6742BXAAAA	N6742B - 16+1 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event),EP3C16, SE	NIM
WV1742XAAAAA	V1742 - 32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	6U-VME64
WV1742BXAAAA	V1742B - 32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/events), EP3C16, SE	6U-VME64
WVX1742XAAAA	VX1742 - 32+2 Ch. 12 bit 5 GS/s Switched-Capacitor Digitizer: 128 events/ch (1kS/event), EP3C16, SE	6U-VME64X
WVX1742BXAAA	VX1742B - 32+2 Ch. 12 bit 5GS/s Switched-Capacitor Digitizer: 1024 events/ch (1kS/event), EP3C16, SE	6U-VME64X

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

APPLICATIONS

- Nuclear and Particle Physics
- Astroparticle Physics
- Time of Flight
- Medical Imaging (PET)

FORM FACTOR

VME64 VME64X NIM DESKTOP

FEATURES

USB Digital I/O Optical Link

Based on the SAMLONG, a Switched Capacitor Array

Fast Switched Capacitor Digitizer with self trigger and charge integration

743 Digitizer Family

16/8 Ch. 12-bit 3.2 GS/s Digitizer

Overview

The 743 is a family of 12-bit and 3.2 GS/s Switched Capacitor Waveform Digitizers with 2.5 Vpp of input dynamic range and DC offset adjustment, issued from the collaboration with CEA/IRFU & CNRS/IN2P3/LAL and based on the SAMLONG chip.

It is available in three form factors: VME (16 input channels), NIM (8 input channels) and Desktop (8 input channels).

Considering the sampling frequency and the number of bits, these digitizers are well suited for very fast signals as the ones coming from fast scintillators coupled to PMTs, Silicon Photomultipliers, APD, Diamond detectors and others.

The analog input signals are continuously sampled inside the SAMLONG chip in a circular memory buffer (1024 cells) at the default sampling frequency of 3.2 GS/s (312.5 ps of sampling period); 1.6, 0.8 or 0.4 GS/s frequencies can also be selected. As a trigger signal arrives, all analog memory buffers are frozen and subsequently digitized with a resolution of 12 bits into a digital memory buffer with independent read and write access. Up to 7 full events per channel can be stored where 1 event is made of 1024 samples.

During analog to digital conversion process, the x743 digitizer cannot handles other triggers, thus generating a Dead Time.

A common acquisition trigger signal can be provided externally via front panel digital input connector or via software. Alternatively each channel is equipped with a discriminator, with programmable threshold, generating trigger requests. The requests from the enabled channels are processed by the board to generate a common trigger causing the event to be stored simultaneously (for all enabled channels). These requests are also used by counters to continuously calculate the individual channel hit rates, also during the Dead Time. The trigger from one board can be provided on a front panel digital output connector.

Firmware	Software	Features
WAVEFORM RECORDING	CAEN WAVECATCHER	Digital Waveform Recorder Charge Integration Constant Fraction Discrimination

Each channel is equipped with an individual fixed amplitude pulser for test and reflectometry applications. An on-board charge mode option can be enabled for charge calculation and fast histogramming.

743 family supports multi-board synchronization making a multi-board system where all ADCs result to be synchronized to a common clock source, and ensuring Trigger Time Tag alignment. Once synchronized, all data will be aligned and coherent across multiple x743 boards.

Features

- 12-bit @ 3.2 GS/s, 1024 samples per event
- 3.2, 1.6, 0.8, 0.4 GS/s software selectable sampling frequencies
- Analog inputs on MCX coaxial connectors
- VME64/VME64X (16 ch.), NIM (8 ch.) and Desktop (8 ch.) modules
- 2.5 Vpp input dynamic range with programmable DC offset adjustment
- One discriminator per channel with programmable threshold
- Adjustable post-trigger delay (up to 1.25 µs @ 3.2 GS/s)
- One embedded pulser per channel for test and reflectometry applications
- On-board charge calculation for fast histogramming
- VME, USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Oscilloscope software tool, C and LabVIEW libraries

x743 is based on the SAMLONG, a Switched Capacitor Array. This technology relies on a set of capacitors that continuously sample the analog input signals at a fixed time interval which corresponds to the sampling period. When the trigger is issued, capacitors are decoupled from the input signals after a programmable delay. The trigger therefore freezes the currently stored signal in the sampling capacitance cells. Subsequently the cells are multiplexed into the 12-bit ADC.

x743 features an embedded Charge Mode, where the pulse integration window is defined by the user. This feature allows to perform on-line processing on detector signal directly digitized.

Technical Specifications

GENERAL

Form Factor
1-unit wide, 6U VME64/VME64X
1-unit wide NIM
154x50x164 mm³ (WxHxD) Desktop

ANALOG INPUT

Channels
16 channels, single ended (VME)
8 channels, single ended (NIM, Desktop)

Impedance
50 Ω

Connector
MCX

Full Scale Range (FSR)
2.5 Vpp

Bandwidth
500 MHz

Offset
Programmable DAC for DC offset adjustment.
Range: ±1.25 V

DIGITAL CONVERSION

Switched Capacitor array
SAMLONG fast analog memory chip serving 2 channels
1024 storage cells per channel (320 ns minimun recorded time per event)

Resolution
12 bits

Sampling rate
3.2 (default) - 1.6 - 0.8 - 0.4 GS/s software selectable, simultaneously on each channel

Dead Time for Event A/D conversion
125 µs (max. @1024 samples)

CLOCK GENERATION

Synchronization clock source: internal/external
On-Board PLL provides generation of main board clocks from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference

MEMORY

7 events/ch (1024 samples per event) Multi-Event Buffer

TRIGGER

Trigger source
Self-trigger: channel over/under threshold (based on individual discriminator with DAC adjusted threshold) for Common trigger generation
External-trigger: Common by TRG-IN connector
Software-trigger: Common by software command

Trigger propagation
TRG-OUT (VME) / GPO (NIM and Desktop) digital output

Trigger Time Stamp
40-bit counter, 5 ns resolution, 90 minutes range (@ 3.2 GS/s)

LVDS I/O (VME only)

16 general purpose LVDS I/Os controlled by FPGA
Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed An Input Pattern from the LVDS I/Os can be associated to each trigger as an event marker

SYNCHRONIZATION

Clock propagation
Daisy chain (VME only) through CLK-IN/CLK-OUT connectors
One-to-many clock distribution from an external clock source Clock Cable delay compensation

Acquisition Synchronization
Sync Start/Stop through digital I/O (S-IN, TRG-IN or GPI input, TRG-OUT or GPO output)
External Trigger Time Stamp reset

COMMUNICATION INTEFRACE

Optical Link
CAEN CONET proprietary protocol, up to 80 MB/s transfer rate
Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)

USB (NIM and Desktop direct, VME via V1718 bridge)
USB 2.0 compliant
Transfer rate up to 30 MB/s

VME
VME 64X compliant
Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

POWER CONSUMPTIONS

Desktop: 1.5 A @ 12 V (Typ.)
NIM: 2.9 A @ +6 V, 500 mA @ -6 V
VME: 4 A @ +5 V, 625 mA @ +12 V, -12 V not used

Ordering Options

Code	Description	Form Factor
WDT5743XAAAA	DT5743 - 8 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 7 events/ch (1kS/event), EP3C16, SE	Desktop
WN6743XAAAAA	N6743 - 8 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 7 events/ch (1kS/event), EP3C16, SE	NIM
WV1743XAAAAA	V1743 - 16 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 7 events/ch (1kS/event), EP3C16, SE	6U-VME64
WVX1743XAAAA	VX1743 - 16 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 7 events/ch (1kS/event), EP3C16, SE	6U-VME64X

Accessories

A2818
PCI CONET Controller

A3818
PCI Express CONET2 Controller

A654
MCX to LEMO Cable Adapter

A659
MCX to BNC Cable Adapter

A317
Clock Distribution Cable

A318
SE to Differential Clock Cable Adapter

AI2700
Optical Fiber Series

Cables for CONET Optical Link Networks

Acquistion Modes

Firmware and Sofware Selection

Thanks to their flexibility, CAEN Digitizers can be operated as pure waveform recorders or can run special algorithms to process the digitized pulses and extract a set of significant information like energy, pulse shape and precise timing.

Each acquisition mode makes use of a specific firmware and software to tailor the digitizer capabilities to the user's needs.

Hardware

Firmware

Waveform Recording Firmware

- *Time windowed waveform recording*
- *Dead-timeless acquisition*
- *Multi-buffer memories*
- *Multi-board synchronization*
- *High bandwidth data readout*

Digital Pulse Processing (DPP) Firmware

- **DPP DAW** — Dynamic Acquisition Window
- **DPP ZLE PLUS** — Zero Lenght Encoding
- **DPP PHA** — Pulse Height Analysis
- **DPP QDC** — Charge to Digital Conversion
- **DPP PSD** — Gated Charge Integration and Pulse Shape Discrimination

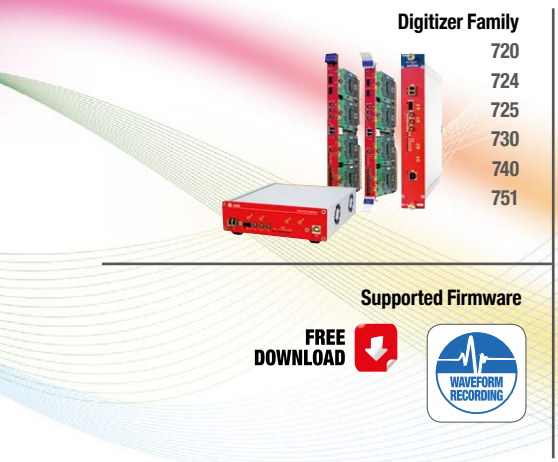
Software

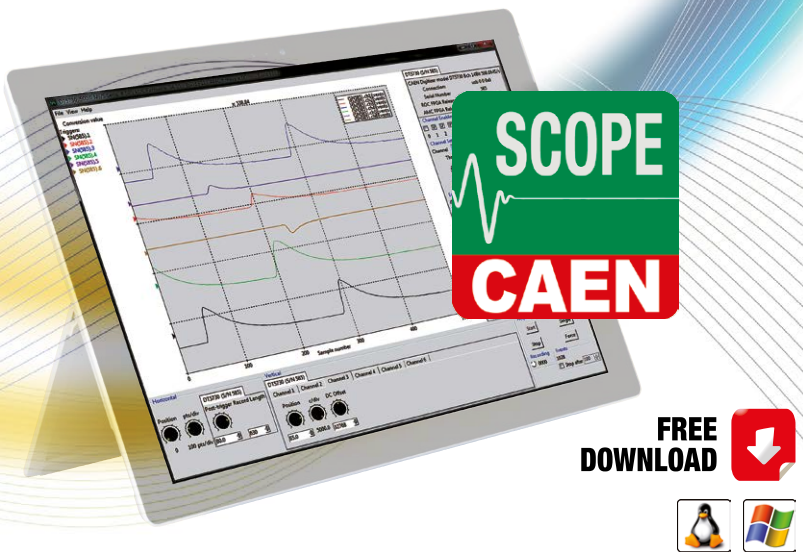
Waveform Recording Software

- **SCOPE CAEN** — Signal Inspection and Waveform Recording Software
- **WAVE DUMP CAEN** — Open Source Acquisition Software for Developers
- **CAEN WAVECATCHER** — Advanced Software Tool for 743 Digitizers

DPP Software

- **CoMPASS CAEN** — Multiparametric DAQ Software for Physics Applications
- **MC² CAEN** — User Friendly Software for DPP-PHA Management
- **PSD CAEN** — Graphical Interface for DPP-PSD Management
- **QDC CAEN** — Demo Software for DPP-QDC Management
- **ZLE+ CAEN** — Demo Software for DPP-ZLEplus Management
- **DAW CAEN** — Demo Software for DPP-DAW Management





Waveform Recording

CAENScope
Signal Inspection and Waveform Recording Software

Overview

CAENScope is a user friendly software interface to specifically control CAEN digitizer running "Default Firmware" (waveform recording).

CAEN Scope allows the user to easily connect to a single board, retrieve the hardware information, manage the acquisition and data recording.

In a single program frame, different parameters can be set for the channels, the trigger (e.g. external, software or channel trigger) and the traces (e.g. vertical and horizontal digital settings, and hardware settings as well). Up to 12 traces can be simultaneously plotted.

A wave recording session can be programmed even by number of events and then saved to files in a Binary (SQLite db) or Text (XML) format. It is possible to load a recorded session and have it on the display with the recording date and the trace from each enabled channel, scrolling it event by event. The user can also export and import the software settings at his convenience.

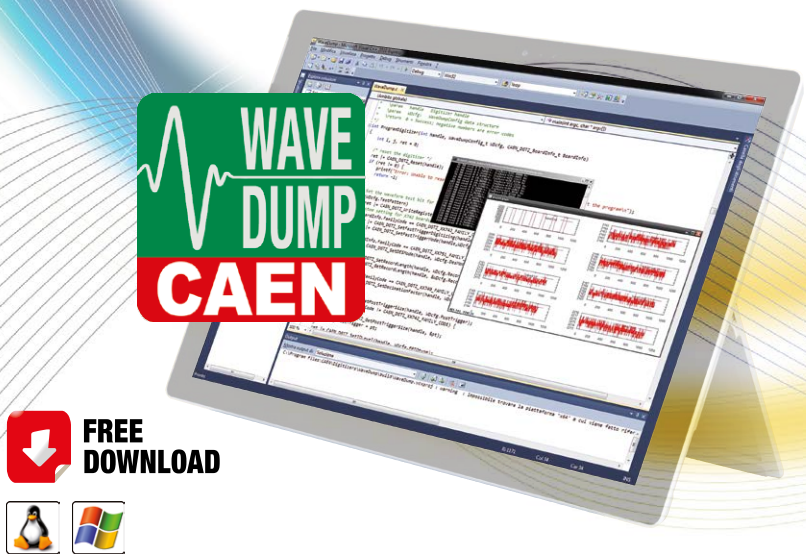
Features

- User friendly single frame GUI with intuitive controls
- Compatible with CAEN Waveform Digitizers
- Extended plot and record capability up to 12 simultaneous traces
- High configuration flexibility:
  - individual channel enable/disable
  - individual channel trigger threshold and DC offset adjustment
  - common trigger among channels
  - external trigger enable/disable
  - auto trigger
- Multi format (ASCII, binary) data saving
- Import/Export of recorded waveform and software settings
- Compliant with Windows and Linux platforms

Applications

- Signal inspection and waveform recording
- Research and development of prototypes
- Data collection for offline statistical analysis
- Beam monitoring
- Sensors readout and detectors' performances
- Lidar

Features	Firmware	Software	Digitizer Family	Max Sampling Rate (MS/s)	Resolution (bits)	Channels
Digital Waveform Recorder	WAVEFORM RECORDING	SCOPE CAEN	720	250	12	8/4/2
			724	100	14	8/4/2
			725	250	14	16/8
			730	500	14	16/8
			740	62.5	12	64/32
			751	1000-2000	10	8-4/4-2



FREE DOWNLOAD

Digitizer Family

720 724
725 730
740 742
751 761

Supported Firmware

WAVEFORM RECORDING

FREE DOWNLOAD

WaveDump

Open Source Acquisition Software for Developers

Waveform Recording

Features

- Basic console for waveforms acquisition
- Compliant with CAEN digitizers
- Multichannel waveform plot
- Advanced mode configuration:
  - common board settings
  - individual settings for threshold and DC offset adjustment
  - 725-730-751 ADC calibration
- Advanced mathematical functions: amplitude spectra and FFT
- Configuration of 742 boards and DRS4 chip corrections
- Multi format (ASCII, binary) data saving
- Source files and Visual Studio project open source for developers

Overview

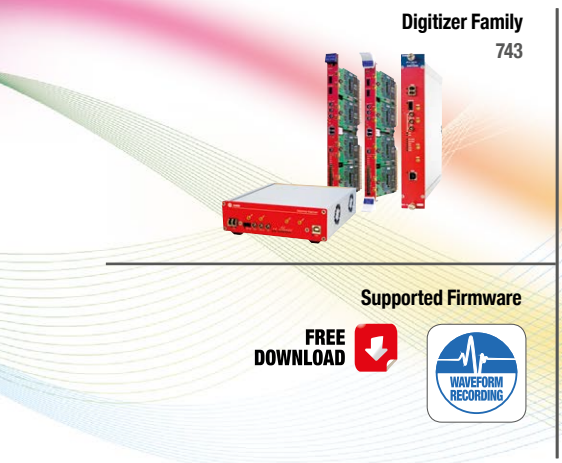
WaveDump is a basic console application supporting digitizers running default firmware. WaveDump allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition. It is then possible to read the data, display the readout and trigger rate. Moreover, it is also possible to apply some post-processing (e.g. FFT and amplitude histogram), save data into a file and also plot the waveforms using Gnuplot third-party graphical utility.

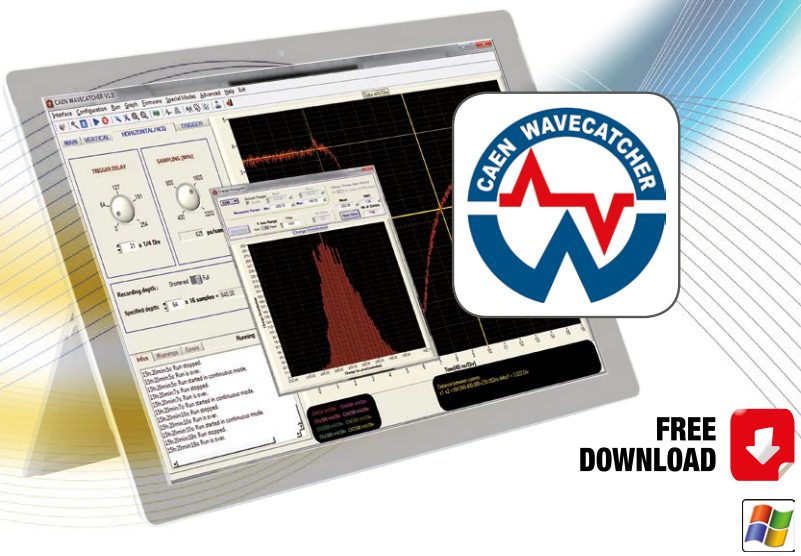
WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Expert users can start with this demo to write their own acquisition software to exploit the full potentialities of the digitizers. Source files and the VS project are available for free download.

Applications

- Signal inspection and waveform recording
- Research and development of prototypes
- Data collection for offline statistical analysis
- Beam monitoring
- Sensors readout and detectors' performances
- Lidar

Features	Firmware	Software	Digitizer Family	Max Sampling Rate (MS/s)	Resolution (bits)	Channels
Digital Waveform Recorder	WAVEFORM RECORDING	WAVE DUMP CAEN	**720**	250	12	8/4/2
			724	100	14	8/4/2
			725	250	14	16/8
			730	500	14	16/8
			740	62.5	12	64/32
			742	5000	12	32+2/16+1
			751	1000-2000	10	8-4/4-2
			761	4000	10	2/1





Waveform Recording

WaveCatcher
Advanced Software Tool for 743 Digitizers

Overview

The WaveCatcher software and the default firmware for 743 family is a complete oscilloscope-like tool made by CNRS/IN2P3/LAL, which is able to control a single board belonging to the CAEN 743 Digitizer series.

A graphical user friendly interface is available to take benefit of all the functions of the hardware: sampling frequency, different trigger modes, waveforms and charge data acquisition, channel pulses, etc.

The system also features different tools for on-line measurements and histograms plotting: graphical cursors, noise level, raw hit rates, charge amplitude and time measurements, time distance histograms between channels (fixed threshold and digital CFD methods), charge histograms, FFT, etc.

All acquired data and computed measurements can be saved to files for further off-line analysis.

Features

- Software by CNRS/IN2P3/LAL to control x743 digitizers
- Single-board communication and data acquisition management
- Friendly Graphical User Interface for board configuration and on-line measurements setting
- Waveforms, charge and time histograms advanced plotting
- Advanced menu for Rate, Noise and Time measurements
- Saving and recalling options for configuration parameters and data
- Data saving (waveforms and/or measurements) in ASCII and Binary file formats for storage or off-line analysis
- Compliant with Windows OS and Linux (Coming Soon)

Applications

- Signal inspection and waveform recording
- Research and development
- Precise Timing for Time of Flight measurements
- Lidar

Features	Firmware	Software	Digitizer Family	Max Sampling Rate (MS/s)	Resolution (bits)	Channels
Digital Waveform Recorder **Charge Integration** **Constant Fraction Discrimination**	WAVEFORM RECORDING	CAEN WAVECATCHER	**743**	3200	12	16/8

Digitizer Family
720 724
725 730
740 751

Supported Firmware

DPP QDC | DPP PHA | DPP PSD

FREE TRIAL VERSION

FREE DOWNLOAD

NEW CoMPASS
Multiparametric DAQ Software for Physics Applications

Digital Pulse Processing

Features

- Software for simultaneous DPP acquisition, including Pulse Height Analysis (PHA)[2], Pulse Shape Discrimination (PSD), Charge Integration (CI)[1], and the new digital QDC[3]
- Multi-board management
- Synchronization of multiple boards even from different families
- Correlation between different channels
- Simultaneous plot of waveform, energy, time, PSD, and TOF spectra
- Energy calibration
- Digital Constant Fraction Discrimination for fine time stamp interpolation (pico second intrinsic resolution)
- Selectable filters on energy, PSD, and Correlation
- Advanced data saving options:
  - Data from board is recorded for the whole acquisition run
  - Time ordered recording of channels acquired data (list mode)
  - Spectra saving
- Data can be retrieved offline to make additional filters and analysis
- ROOT format data saving (Coming Soon)
- Add-on for ROOT integration (Coming Soon)

Overview

CAEN **M**ulti-**PA**rameter **S**pectroscopy **S**oftware (**CoMPASS**) is the new software from CAEN able to implement a Multi-parametric DAQ for Physics Applications, where the detectors can be connected directly to the digitizers inputs and the software acquires energy, timing, and PSD spectra.

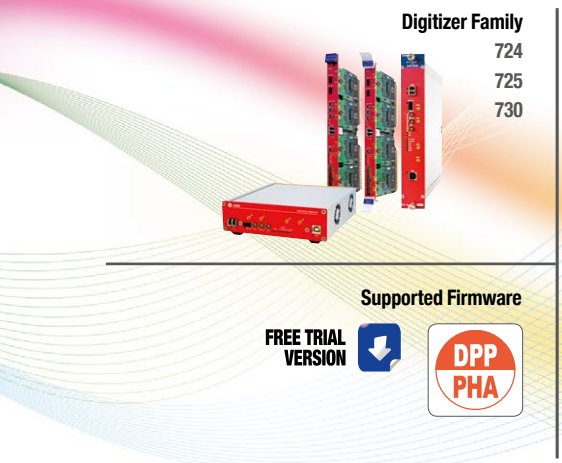
CoMPASS can manage multiple boards, even in synchronized mode, and the event correlation between different channels (in hardware and/or software), apply energy and PSD cuts, calculate and show the statistics (trigger rates, data throughput, etc…), save output data files (raw data, lists, waveforms, spectra) and use the saved files to run off-line with different processing parameters.

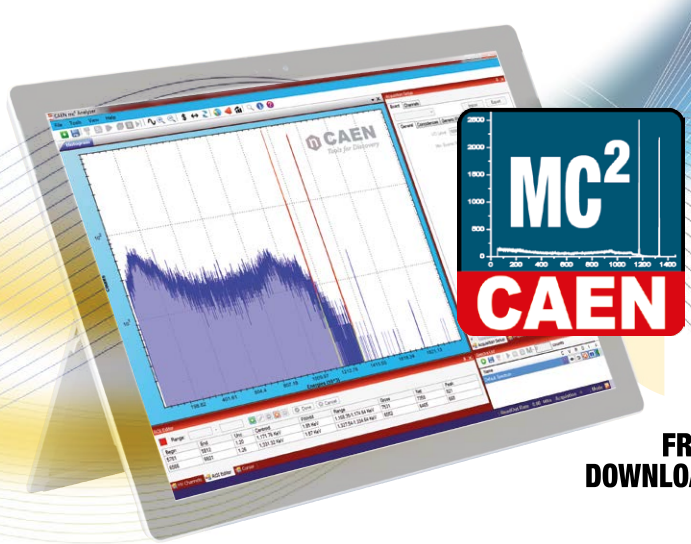
Applications

- Nuclear spectroscopy
- Clover detectors
- HPGe, Silicon Drift Detectors
- Neutron physics with scintillation detectors
- Multiple boards synchronization
- Homeland security
- Precise Timing for Time of Flight measurements

Features	Firmware	Software	Digitizer Family	Max Sampling Rate (MS/s)	Resolution (bits)	Channels
Charge Integration Pulse Shape Discrimination	DPP PSD	CoMPASS CAEN	720[1]	250	12	8/4/2
Charge Integration Pulse Shape Discrimination Constant Fraction Discriminator	DPP PSD	CoMPASS CAEN	725	250	14	16/8
			730	500	14	16/8
			751	1000-2000	10	8-4/4-2
Pulse Height Analysis	DPP PHA	CoMPASS CAEN	724[2]	100	14	8/4/2
			725	250	14	16/8
			730	500	14	16/8
Digital QDC Charge Integration	DPP QDC	CoMPASS CAEN	740[3]	62.5	12	64/32

(1) DPP-CI is no longer supported. To perform Charge Integration please refer to the DPP-PSD
(2) DPP-PHA firmware is no longer supported for 724 models with C4 AMC FPGA option
(3) CoMPASS support of DPP-QDC: Coming Soon





FREE DOWNLOAD

Digital Pulse Processing

MC²Analyzer
User Friendly Software for Digital Pulse Height Analysis

Overview

MC²Analyzer is a software specifically designed to manage CAEN Digital MCA (780/781 family, DT5770, and gamma *stream*) as well as CAEN digitizers running DPP-PHA (Digital Pulse Processing for the Pulse Height Analysis) firmware, like 724, 725 and 730 families.

The DPP-PHA firmware implements a digital trapezoidal filter on the input pulse, which replaces the traditional analog chain of shaping amplifier and peak sensing ADC. The MCA is therefore directly connected to the charge sensitive preamplifier, with no need of additional devices. The PHA algorithm is able to perform online baseline restoration, ballistic effect corrections, and manage the pile-up for the live time information. PHA and time-stamped list acquisition modes are available.

MC²Analyzer software allows the user to program the relevant DPP-PHA parameters, to manage the HV channels configuration (x780 and gamma *stream* only), to collect the spectra and perform mathematical analysis, like energy calibration, peak search, background subtraction, peak fitting, etc.

The software is designed with multi-channel and multi-board capabilities: it can handle several boards and manage the data acquisition from each of them at the same time.

COMING SOON

Features

- Designed for:
  - 724, 725 and 730 Digitizer families
  - 770/780/781 Digital MCA families and gamma *stream*
- Trapezoidal filter replacing shaping amplifier and peak sensing ADC
- Online baseline restoration and ballistic effect correction
- Online pile-up correction for live-time measurement
- PHA and time-stamped list mode available
- Full setting of all the relevant DPP-PHA parameters and power supplies for DT5780 and gamma *stream* controlled by the MC²Analyzer software
- Complete simultaneous control of different boards
- Advanced mathematical analysis on collected spectra (peak search, background subtraction, peak fitting, etc.)
- Provides Energy, Time Stamp lists and histograms in ASCII and ANSI N42.42 format (energy spectra for 770 only)

Applications

- Nuclear spectroscopy
- HPGe, silicon drift, silicon strip detectors
- Slow scintillation detectors (i.e. NaI(Tl))
- Anti-compton shielding
- Homeland security
- Environmental survey
- Ion beam analysis
- Nuclear medicine

Ordering Option

Code	Description
WFWDPPTFAA25	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (x725)
WFWDPPTFAA30	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (x730)
WFWDPPTFAAAA	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (x724)

Features	Firmware	Software	Digitizer Family	Max Sampling Rate (MS/s)	Resolution (bits)	Channels
Pulse Height Analysis	DPP PHA	MC² CAEN	724(1)	100	14	8/4/2
			725	250	14	16/8
			730	500	14	16/8

(1) DPP-PHA firmware is no longer supported for 724 models with C4 AMC FPGA option

FREE DOWNLOAD

Digitizer Family
720
725
730
751

Supported Firmware

DPP PSD

FREE TRIAL VERSION

NEW DPP-PSD
Digital Charge Integration and Pulse Shape Analysis

Digital Pulse Processing

Features

- Digital solution equivalent to Dual Gate QDC + Discriminator + Gate Generator
- Double charge integration for Pulse Shape Discrimination
- Single gate integration for Energy spectra calculation
- Self Gating (no discriminator) with digital noise filtering
- No delay line is needed to fit the position of the pulse inside the gate
- Programmable width and position of the two gates
- Automatic Baseline subtraction (pedestal)
- Digital Constant Fraction Discrimination for fine time stamp interpolation (pico second intrinsic resolution)
- Dead-timeless acquisition (no conversion time)
- On-line coincidences/anti-coincidence acquisition mode among channels
- Extremely high dynamic range
- Provides also timing information (pulse time stamps)
- Free downloadable firmware trial version
- Demo software to handle digitizer families running DPP-PSD firmware

Applications

- Spectroscopy with scintillation organic/inorganic detectors
- SiPM readout systems
- Neutron physics with liquid scintillation detectors
- Acquisition from phoswich detectors
- Time dependent spectroscopy
- Precise timing for Time of Flight measurements
- Homeland security
- Neutron imaging
- PET
- Tagged neutron for inspection systems

Overview

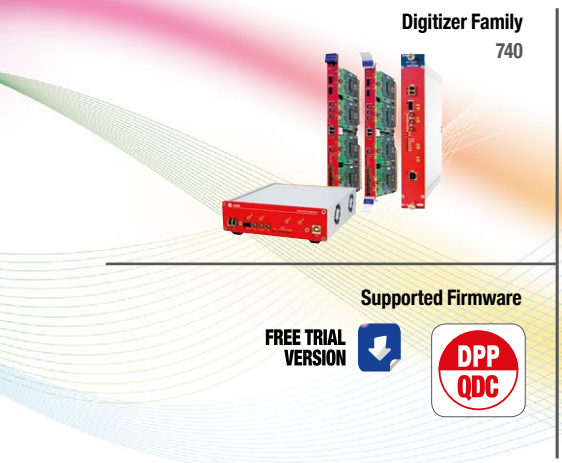
A digitizer running the DPP-PSD firmware becomes a multichannel data acquisition system for nuclear physics or other applications requiring radiation detectors. The digitizer accepts signals directly from the detector and implements a digital replacement of Dual Gate QDC, Discriminator and Gate Generator. All these functions are performed inside the board FPGA without any use of external cables, nor additional boards or delay lines. The acquisition is therefore performed by a single compact system which replaces the traditional analog boards. It is also possible to operate with multi-board systems: the front panel clock, the trigger and the general purpose LVDS I/Os connectors (VME only) make possible the synchronization of several boards.

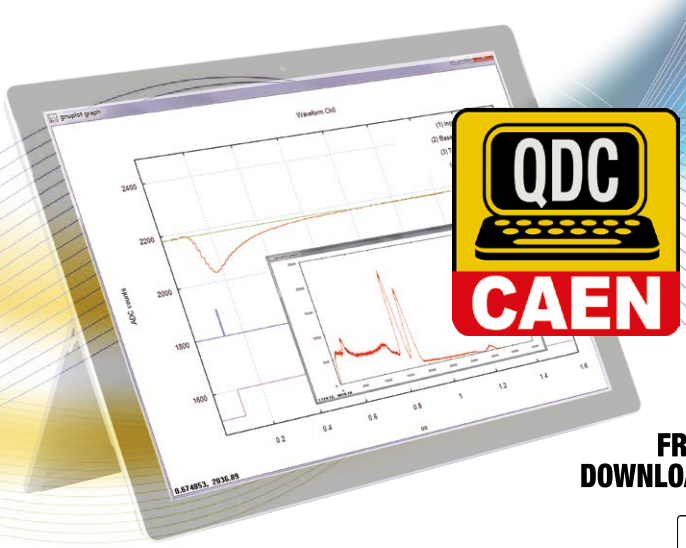
The acquisition can be controlled by the DPP-PSD Control Software, a demo program that allows the user to understand the principle of operation of the DPP-PSD algorithm, program the digitizer and control the acquisition and data saving.

Ordering Option

Code	Description
WFWDPPNGAA20	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x720)
WFWDPPNGAA25	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x725)
WFWDPPNGAA30	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x730)
WFWDPPNGAA51	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (x751)

Features	Firmware	Software	Digitizer Family	Max Sampling Rate (MS/s)	Resolution (bits)	Channels
Charge Integration Pulse Shape Discimination	DPP PSD	PSD CAEN	720	250	12	8/4/2
Charge Integration Pulse Shape Discrimination Constant Fraction Discriminator	DPP PSD	PSD CAEN	725 730 751	250 500 1000-2000	14 14 10	16/8 16/8 8-4/4-2





FREE DOWNLOAD

Digital Pulse Processing

DPP-QDC
Digital Charge to Digital Converter for 740 Digitizers

NEW

Overview

Tired of your old QDC? Try the new digital QDC algorithm for 740 digitizer series. Digital QDC is specifically supported by x740D models mounting EP3C40 Altera FPGA. 740D digitizer series running DPP-QDC firmware become multi-channel data acquisition systems for nuclear physics or other applications requiring radiation detection. The digitizers accept signals directly from the detector and implement a digital replacement of Single Gate QDC, Discriminator and Gate Generator.

The algorithm is able to self-trigger up to 32/64 channels independently, according to the board form factor. Furthermore, the trigger filter of each channel can be programmed independently to allow for a fine tuning of the threshold. The integration gate itself can be programmed independently to get the best resolution from different detector systems.

The new digital QDC is able to self gate on the input pulse with no need of additional delay lines, nor external discriminator.

It is particularly suitable for segmented detector configuration, where multiple channels need to be acquire simultaneously.

CAEN provides open source demo software for a first approach to DPP-QDC algorithm principles and basic control of the digitizer.

Ordering Option

Code	Description
WFWDPPQDCAAA	DPP-QDC- Digital Pulse Processing for Time Stamped Digital QDC (x740)

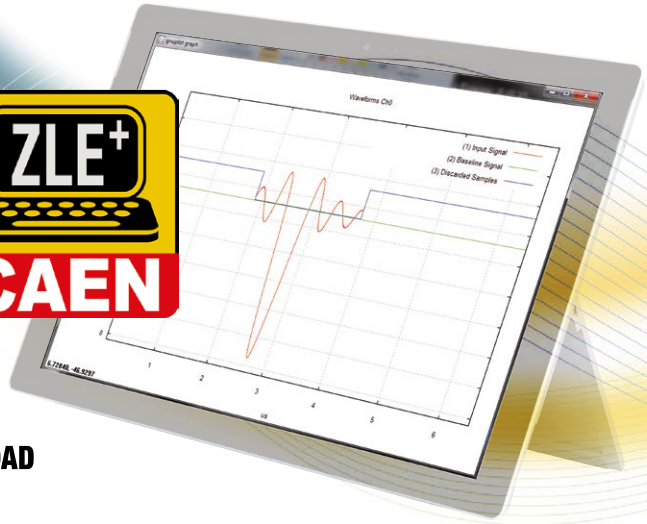
Features

- Digital solution equivalent to Single Gate QDC + Discriminator + Gate Generator
- **Runs only on x740D models**
- Single gate integration for Energy spectra calculation
- Self-Gating (no discriminator) with digital noise filtering
- No delay line is needed to fit the position of the pulse inside the gate
- Independent 32 (Desktop, NIM) - 64 (VME) channel self-trigger
- Trigger adjustment for single channel
- Programmable gate width and position for single channel
- Automatic Baseline subtraction (pedestal)
- Dead-timeless acquisition (no conversion time)
- Provides also timing information (pulse time stamps)
- Free downloadable firmware trial version
- Demo software to handle 740 digitizer family running DPP-QDC firmware

Applications

- Spectroscopy with scintillation detectors, as NaI(Tl), $LaBr_3$(Ce), $CeBr_3$
- Suitable for applications with detector arrays
- Homeland security
- Environmental survey
- Compton camera

Features	Firmware	Software	Digitizer Family	Max Sampling Rate (MS/s)	Resolution (bits)	Channels
Digital QDC **Charge Integration**	DPP QDC	QDC CAEN	**740**	62.5	12	64/32



FREE DOWNLOAD

Digitizer Family
725
730
751

Supported Firmware

DPP ZLE PLUS

FREE TRIAL VERSION

DPP-ZLEplus
Advanced Zero Length Encoding

Digital Pulse Processing

Features
- Input signal baseline calculation channel by channel
- Acquisition window generated by an external trigger
- Enhanced Zero Suppression of input signals within the acquisition window
- Upper and Lower Threshold referred to the baseline or to an absolute value
- Programmable Look Back and Look Ahead windows
- Provides also timing information (trigger time stamps)
- Demo software to handle 751 digitizer family running DPP-ZLEplus firmware
- Data plotting using Gnuplot graphical engine
- Source files and Visual Studio project provided for developers

Applications
- Neutrino experiments
- Large number of detectors driven by an external trigger
- Drift chambers, TPC, Cherenkov detectors
- Application requiring an effective data reduction

Overview
The Zero Length Encoding (DPP-ZLEplus) firmware has been developed for the 751 digitizer family (725-730 Coming Soon). It allows the user to transfer the digitized waveforms in compressed mode, performing an enhanced Zero Suppression algorithm on the input signals.

DPP-ZLE continuously calculates the baseline of the input signals and, whenever an external trigger occurs, it searches for the significant input pulses within an user-defined acquisition window. An input pulse is considered significant if it either exceeds an Upper Threshold or falls below a Lower Threshold referred either to the calculated baseline or absolute values.

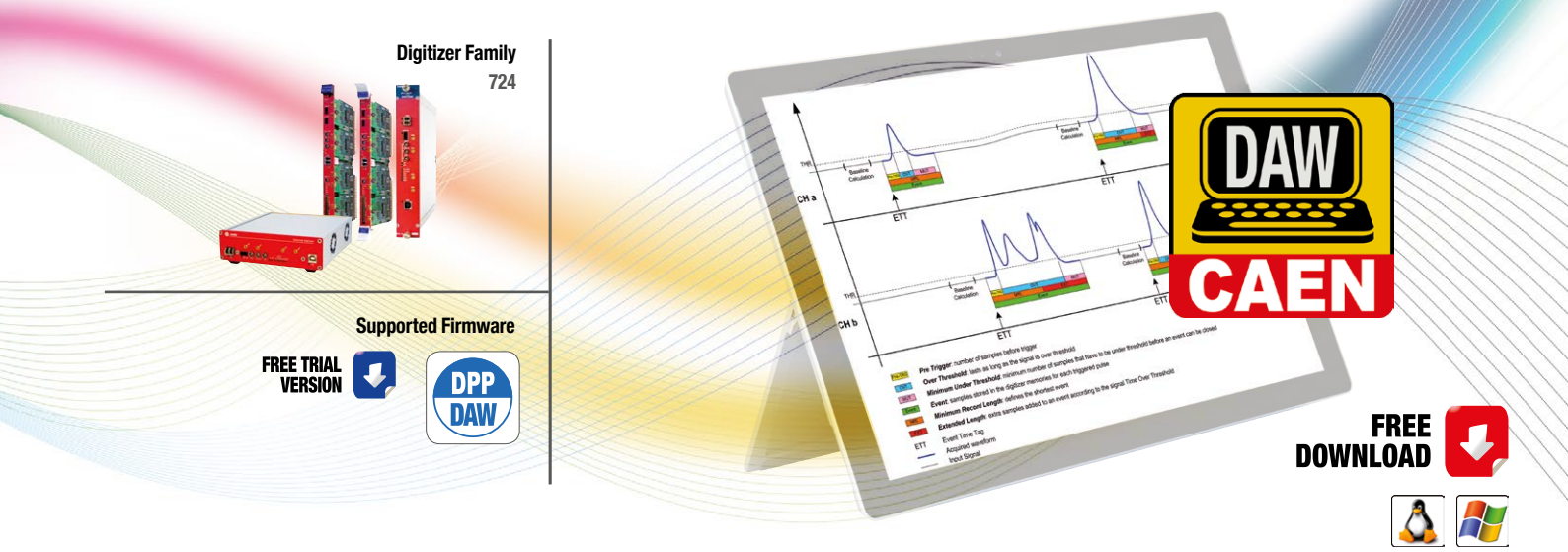
CAEN provides open source demo software for a first approach to DPP-ZLEplus algorithm principles and basic control of the digitizer.

Ordering Option

Code	Description
WFWDPPZLAA51	DPP-ZLE - Digital Pulse Processing Zero Length Encoding for (x751)

Features	Firmware	Software	Digitizer Family	Max Sampling Rate (MS/s)	Resolution (bits)	Channels
Digital Waveform Recorder with Enhanced Zero Suppression	DPP ZLE PLUS	ZLE+ CAEN	**725**(1)	250	14	16/8
			730(1)	500	14	16/8
			751	1000-2000	10	8-4/4-2

(1) DPP-ZLE for x725 and x730: Coming Soon



Digital Pulse Processing

DPP-DAW - Channel Independent Zero Suppression with Dynamic Acquisition Window

NEW

Overview

The Dynamic Acquisition Window (DPP-DAW) firmware has been developed to improve the zero suppression capabilities of the CAEN 724 digitizer family and allow for trigger-less acquisition systems.

By running DPP-DAW firmware, each 724 digitizer channel is able to self-trigger and acquire data independently from the others.

DPP-DAW can dynamically adjust the record length of every triggered event according to its Time Over Threshold to fit the actual duration of the input pulses. This prevents that a pulse larger than the expected gets chopped because of a too short acquisition window.

DPP-DAW is able to continuously evaluate the signal baseline and refer a trigger threshold to its value. Therefore, the threshold can follow the baseline drift of the input signal without changing the trigger conditions of the data acquisition system.

The user can set a minimum record length, a pre-trigger and a minimum not to lose those samples of interest before and after the Time Over Threshold. This allows for a full reconstruction of the digitized pulses.

DPP-DAW can accept an external veto to inhibit the data acquisition. A programmable input delay is available to compensate for the latency due to the veto generation if managed by an external logic unit.

It is possible to store not only the overthreshold part of the significant pulses, but also the samples before and after the threshold crossing points by means of programmable Look Back and Look Ahead windows.

CAEN provides open source demo software for a first approach to DPP-DAW algorithm principles and basic control of the digitizer.

Features

- Independent channel self-trigger
- Automatic adjustment of the acquisition window length to match the actual input pulse duration
- User defined minimum record length and pre-trigger for a complete event reconstruction
- Continuous signal baseline calculation for baseline drift compensation
- Programmable input delay to compensate for veto generation latency
- Channel Trigger Time Tag for event correlation
- Demo software to handle 724 digitizer family running DPP-DAW firmware

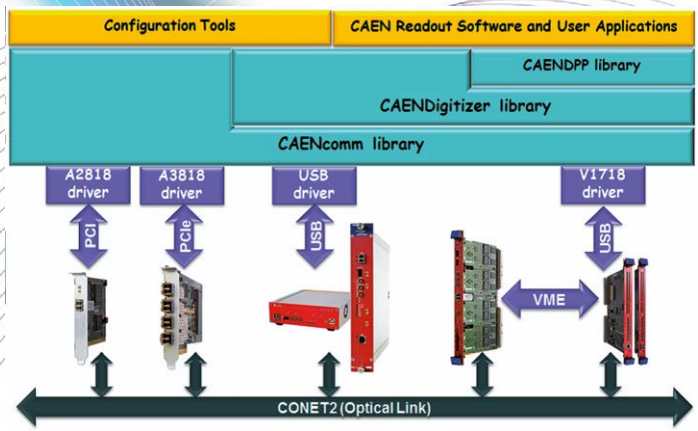
Applications

- Neutrino experiments
- Large number of detectors
- Drift chambers, TPC, Cherenkov detectors
- Application requiring an effective data reduction

Ordering Option

Code	Description
WFWDPPDAWXEA	DPP-DAW - Digital Pulse Processing with Dynamic Acquisition Window (x724)

Features	Firmware	Software	Digitizer Family	Max Sampling Rate (MS/s)	Resolution (bits)	Channels
Digital Waveform Recorder with Zero Suppression for trigger-less acquisition systems	DPP DAW	DAW CAEN	724	100	14	8/4/2



Software Tools

FREE DOWNLOAD

CAEN Comm | CAEN Digitizer | CAEN DPP

CAEN VME Demos | CAEN SyncTest | CAEN Upgrader

Drivers, Libraries and Configuration Tools

CAEN makes available a family of software tools, compliant to Windows and Linux platforms (32-64 bit), to integrate the hardware into the host PC system, to provide the developer with a middle layer for custom programming, to let the user completely and easily configure and retrieve information from a large number of CAEN boards including digitizers:

Drivers

Depending on the physical communication channel:

- USB: USB2.0 compliant
- Optical Link: proprietary CONET protocol managed by A2818 PCI / A3818 PCIe Controllers
- VMEbus: accessed by V1718 / V2718 Bridges

Libraries

C and LabVIEW middleware, including demos and examples for user's development.

Configuration Tools

Friendly software applications for the firmware upgrade or to direct access the board registers for a low level full configuration and control.

Type	Library / Tool name	Firmware type		Programming language	Third-party required software	Supported communication cahnnels	Supported boards
		Digital Pulse Processing Firmware	Waveform recording default firmware				
Library	CAEN Comm	*	*	C, LabVIEW (Windows only)	NI LabVIEW Development System	USB, CONET, VMEbus	VME, NIM and Desktop digitizers, Digital MCAs and DT5790, V65xx power supply boards, V1x90x TDCs, Vx495 general purpose VME board and SY2791 TCP readout system
	CAEN Digitizer	*	*	C, LabVIEW (Windows only)	NI LabVIEW Development System	USB, CONET, VMEbus	VME, NIM and Desktop digitizers[a] , Digital MCAs and Digital Pulse Analyzer DT5790
	CAEN DPP	* (DPP-PHA only)		C		USB, CONET, VMEbus	VME, NIM and Desktop digitizers running DPP-PHA firmware, Digital MCAs
Configuration Tools	CAEN Upgrader	*	*	C, Java	Java Runtime Environment	USB, CONET, VMEbus	VME, NIM and Desktop Digitizers, Digital MCAs and DT5790 , V1x90 TDCs, Vx495, V1718/V2718 VME Bridges, V65xx HV Power Supplies, DT55xx HV Power Supplies, A2818/A3818 PCI/PCIe Controllers, SY2791
	CAEN SyncTest		*	C	Gnuplot (Linux only)	USB, CONET, VMEbus	VME digitizers V1720/V1724/V1740/V1751
	CAEN VME Demos	*	*	C/C++, LabVIEW (Windows only)	Microsoft.NET framework, LabVIEW Run-Time Engine	USB, CONET, VMEbus	VME, NIM and Desktop digitizers, V1718/V2718 VME Brdiges

(a) The LabWIEW library doesn't support 743 digitizer family and DPP-ZLEplus firmware

Libraries

CAENComm

FREE DOWNLOAD

Interface Library for CAEN Data Acquistion Modules

The purpose of the CAENComm library is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer.

CAENComm is based on CAENVMElib, a library developed specifically for USB-VME bridge (Mod. V1718) and PCI-VME (Mod. V2718), which implements the basic functions for accessing the VME bus (besides other specific functions for these bridge). For this reason, it is necessary that the CAENVMELib is already installed on your PC before installing the CAENComm; however, the CAENVMELib is completely transparent to the user.

The library pack includes a ready-to-use demo application, Java and LabVIEW version, including source files as reference for user development.

CAENDigitizer

FREE DOWNLOAD

Library of Functions for CAEN Digitizers High Level Management

CAENDigitizer contains the functions to program CAEN boards like Digitizers, Digital MCAs and Digital Pulse Analyzers, to manage the acquisition, execute the readout, unpack the data, send triggers, etc. This library is designed specifically to support both default and DPP firmware.

CAENDigitizer library relies on the CAENComm and CAEVMELib libraries, allowing to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol. Libraries and applications that rely on the CAENDigitizer become this way independent from the physical layer.

The Library is provided with examples and demo applications, C and LabVIEW version, including source files and sub-VIs as reference for user development.

CAENDPP

FREE DOWNLOAD

High Level Library for CAEN Boards Running DPP Firmware

CAENDPP is a high level library designed to completely control exclusively CAEN digitizers running DPP-PHA firmware and Digital MCAs.

The library allows the user to manage all the relevant board settings, DPP parameters configuration, data acquisition storage. Configuration of synchronized start/stop acquisition is supported in multi-board hardware setup, as well as the single board can be configured for coincidences or anticoincidences among channels. Histograms are built at the library level and managed through specific library functions; other advanced histogram functions are provided (e.g. histogram recovery). Lists of data can be automatically saved to output files. HV management is also handled by the library, if supported by the board.

CAENDPP is provided with examples and Demo applications, including source files, as reference for user development.

Configuration Tools

CAENUpgrader

FREE DOWNLOAD

Firmware Upgrade Tool for Front-end Boards Bridges & VME Power Supply

CAENUpgrader is a software tool with a Java Graphical User Interface (for Windows and Linux OS) to easily upgrade the firmware on a large selection of CAEN boards, such us digitizers and MCAs, bridges and controllers, VME power supply boards. It reunites all the functions included in the cvUpgrade, CAENBridgeUpgrade and PLLConfig CAEN programs, also allowing to configure the PLL settings of VME digitizers (i.e. set the ADC sampling frequency, enable the clock output, etc.), to get the hardware and firmware information and load the license to unlock the pay firmware (e.g. DPP firmware), to control the firmware boot for the NIM and Desktop digitizers.

CAEN VME Demos

FREE DOWNLOAD

Demo Applications for CAEN Bridges Control

CAEN VME Demos are simple programs developed in C/C++ source code and LabVIEW. Versions featuring friendly graphical interfaces are provided for Windows machines.

The demos allow for a full board configuration at low level by direct access (read/write) to the registers. Moreover, they represent a starting point for the development of user-specific applications for CAEN Bridges (V1718/VX1718/V2718/VX2718/A2818/A3818) control.

CAEN SyncTest

FREE DOWNLOAD

Demo Software for CAEN Digitizers Synchronization

CAEN SyncTest is a simple Demo software to demonstrate multi-board synchronization with CAEN VME digitizers running the default firmware. It includes the most relevant commands to adjust the configuration parameters of the boards and read the acquired event data. It represents an example for setting synchronization and trigger distribution, and is provided as an archive of ANSI C source and header files.

SyncTest can be adapted to different synchronization setup and to different VME Dgitizer families.