CAEN Tools for Discovery Electronic Instrumentation

Go

Jobs

V1721

8 Channel 8 bit 500 MS/s Digitizer

- 8 channel
- 1 Vpp input dynamics (single ended or differential)
- 8 bit 500 MS/s ADC
- Analog Sum/Majority and digital over/under threshold flags for Global Trigger logic
- Front panel clock In/Out available for multiboard synchronisation (direct feed through or PLL based synthesis)
- 16 programmable LVDS I/Os
- Trigger Time stamps
- Memory buffer: up to 2 MS/ch
- FPGA for real-time data processing
- Zero Suppression and Data Reduction algorithms
- Programmable event size and pre-post trigger adjustment
- VME64X compliant interface
- Optical Link interface
- A2818 PCI controller available for handling up to 8 Modules daisy chained via Optical Link
- Firmware upgradeable via VME/Optical Link
- Demo software
- Libraries, Demos (C and LabView) and

The Mod. V1721 is a 1-unit wide VME 6U module housing a 8 Channel 8 bit 500 MS/s Flash ADC Waveform Digitizer with threshold Auto-Trigger capabilities. Input dynamics is 1 Vpp (single ended or differential).
The DC offset of the input signal can be adjusted channel per channel by a programmable 16bit DAC on single ended input version.
The modules feature a front panel clock/reference In/Out and a PLL for clock synthesis from internal/external references. This allows multi board phase synchronizations to an external clock reference or to a clock Digitizer master board.
The data stream is continuously written in a circular memory buffer. When the trigger occurs, the FPGA writes further N samples for the post trigger and freezes the buffer that can be read either via VME or via Optical Link. The acquisition can continue without dead time in a new buffer.
Each channel has a **SRAM Multi-Event Buffer** of **2 MS** divisible into **1 ÷ 1024** buffers of programmable size. 'Zero suppression' and 'data reduction'algorithms allow substantial savings in data amount readout and processing, rejecting samples smaller than programmable thresholds.
The trigger signal can be provided via the front panel input as well as via the VMEbus, but it can also be generated internally. The trigger from one board can be propagated to the other boards through the front panel Trigger Output.
An Analog Output allows to reproduce the sum of the input signals as well as the majority of the buffer occupancy.
The Modules VME interface is VME64X compliant and the data readout can be performed in Single Data Transfer (D32), 32/64 bit Block Transfer (BLT, MBLT, 2eVME, 2eSST) and 32/64 bit Chained Block Transfer (CBLT).
The boards houses a daisy chainable Optical Link able to transfer data at 80 MB/s, thus it is possible to connect up to eight ADC boards (64 ADC channels) to a single Optical Link Controller (Mod. A2818). Optical Link and VME access are internally arbitrated.

Package	1-unit wide VME 6U module
Analog Input	8 channels, single-ended (SE) or differential. Input range: 1Vpp; Bandwidth: 250MHz. Programmable DAC for Offset Adjust x ch. (SE only).
Digital Conversion	Resolution: 8 bit; Sampling rate: 200 to 500 MS/s simultaneously on each channel
ADC Sampling Clock generation	Three operating modes: - PLL mode - internal reference (50 MHz loc. oscillator). - PLL mode - external reference on CLK_IN (±100ppm tolerance). - PLL Bypass mode: Ext. clock on CLK_IN drives directly ADC clocks (Freq.: 10 ÷ 500 MHz).
CLK_IN	AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by custom cable).
CLK_OUT	DC coupled differential LVDS output clock, locked to ADC sampling clock. Freq.: 10 ÷ 500MHz.
Memory Buffer	2 MS/ch Multi Event Buffer Divisible into 1 ÷ 1024 buffers Independent read and write access Programmable event size and pre-post trigger
Trigger	Common External TRGIN (NIM or TTL) and VME CommandIndividual channel autotrigger (time over/under threshold)TRGOUT (NIM or TTL) for the trigger propagation to other V1721 boards.
Trigger Time Stamp	32bit - 8ns (34s range). Sync input for Time Stamp alignment
ADC and Memory controller FPGA	One Altera Cyclone EP1C4 per channel
Optical Link	Data readout and slow control with transfer rate up to 80 MB/s, to be used instead of VME bus. Daisy chainable: one A2818 PCI card can control and read eight V1721 boards in a chain.

VME interface	VME64X compliant D32, BLT32, MBLT64, CBLT32/64, 2eVME, 2eSST, Multi Cast CyclesTransfer rate: 60MB/s (MBLT64), 100MB/s (2eVME), 160MB/s (2eSST). Sequential and random access to the data of the Multi Event Buffer. The Chained readout allows to read one event from all the boards in a VME crate with a BLT access.
Upgrade	V1721 firmware can be upgraded via VME or Optical Link
Software	General purpose C Libraries and Demo Programs (CAENScope).
Analog Monitor	12bit / 100MHz DAC FPGA controlled output, four operating modes: Test Waveform: 1 Vpp test ramp generator Majority: MON/Σ output signal is proportional to the number of channels (enabled) under/over threshold (1 step = 125mV) Buffer Occupancy: MON/Σ output signal is proportional to the Multi Event Buffer Occupancy Voltage level: MON/Σ output signal is a programmable voltage level
LVDS I/O	16 gen. purpose LVDS I/O controlled by FPGA Busy, Data Ready, Memory full, Individual Trig-Out and other function can be programmed. An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker.
Input connectors	Single ended: MCX Differential: Tyco MODU II

Code	Description
WV1721BXAAAA	V1721B - 8 Ch. 8 bit 500 MS/s Digitizer: 2MS/ch,C4, DIFF
WV1721XAAAAA	V1721 - 8 Ch. 8 bit 500 MS/s Digitizer: 2MS/ch, C4, SE