CAEN
Tools for Discovery

# 2740/2745

## Digitizer Family

*64-Channel 16-bit 125 MS/s*


open FPGA

16bit 125 MS/s

DESKTOP RACK VME Form Factor

1/10 GbE

USB 3.0

OPTICAL LINK

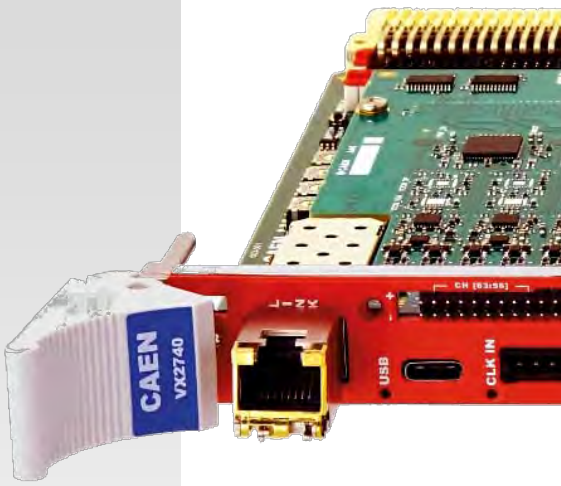
## *The new generation of CAEN Digitizers: Open FPGA and Digital Pulse Processing algorithms for high-density channel experimental setups!*

## Overview

The 2740/2745 Digitizer is a 64-channel digital signal processor for radiation detectors available in VME64 (V2740/V2745), VME64X (VX2740VX2745), and Desktop (DT2740/DT2745) form factor. It offers not only waveform digitization and recording but also Multi-Channel Analysis for nuclear spectroscopy using Silicon strip, segmented HPGe, Scintillation detector with PMTs, Wire Chambers, and others. The 2740/2745 can perform pulse height measurements (PHA), constant fraction timing (CFD), charge integration (QDC) and pulse shape discrimination (PSD) independently for each of the 64 channels. While the 2740 Digitizer is fixed-gain, the 2745 offers a software programmable analog gain up to x100.

## Highlights

- High channel density: 64-channel, 125MS/s 16-bit ADC with individual DC offset adjustment.
- Available in VME64, VME64X and Desktop form factors.
- SW selectable analog gain (2745 only)
- Front panel readout via USB-3.0, 1/10* GbE, optical link (CONET2*)
- 2.5 GB of Total Acquisition memory (DDR4)
- Onboard Zynq® UltraScale+™ MPSoC integrating an Arm®-based CPU running Linux®
- Open FPGA architecture for pulse analysis algorithm customization
- Digital pulse processing and waveform recording of 64 independent detectors
- Advanced waveform readout modes with Zero Length Encoding* (ZLE) or Dynamic Acquisition Window* (DAW)
- Originally designed for Dark Matter Physics applications
- Suitable for Si strip, segmented HPGe, scintillation detectors, and others
- High-resolution Nuclear Spectroscopy: multiport MCA operating in PHA, QDC*, PSD* modes
- Digital CFD* for sub-ns timing measurements
- DAC output (125 MS/s, 2Vpp) for signal inspection, pulse generation, majority level

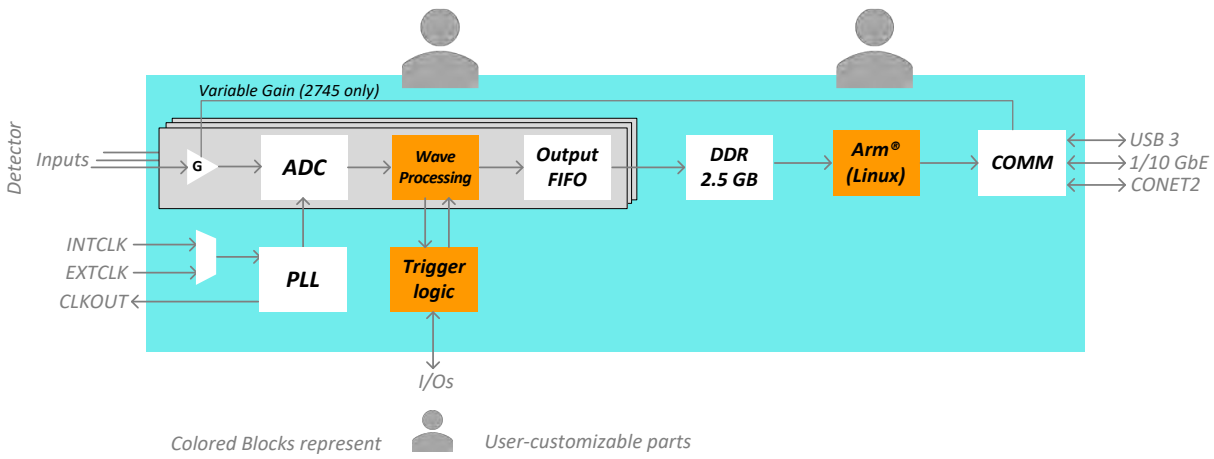



## Software

- User-friendly readout software for multiparametric spectroscopy (CoMPASS*) or waveform recording (WaveDump2)
- Libraries and demo codes available for software customization

*(*) Future Developments*

*2740 / 2745 DIGITIZER ARCHITECTURE*



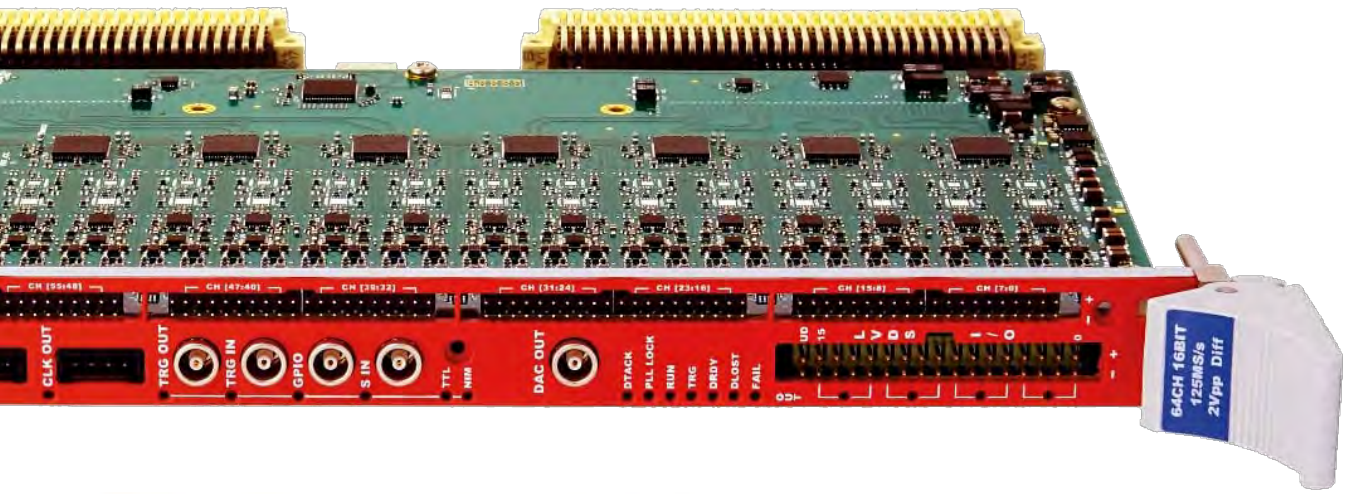
## Operating Modes

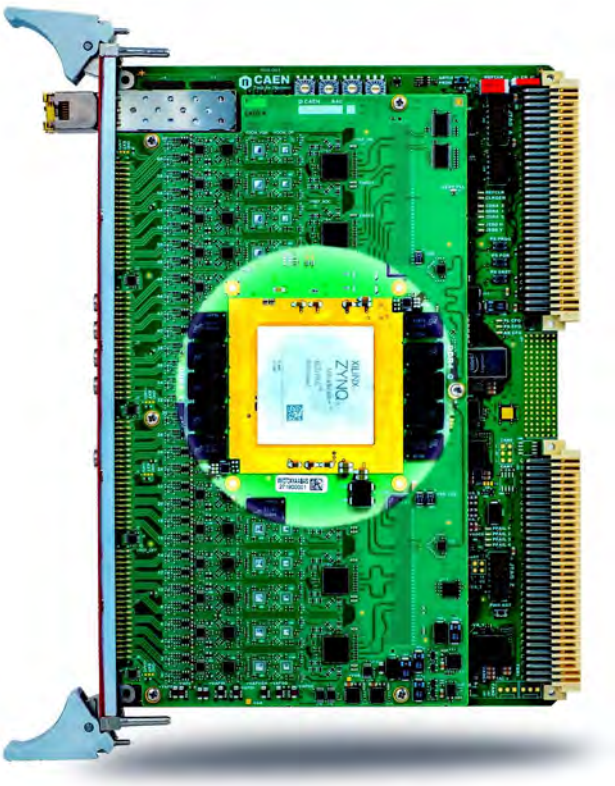
Analog input channels are provided differential (on 2740/2745 versions) or single-ended (on 2740B/2745B versions). Each channel of the module digitizes the analog input, that can be the signal coming from a physics detector, with a 16-bit, 125 MS/s ADC. The sampled data are used to initiate the digital pulse processing sequence, managed in the FPGA at the firmware level. Different firmware types can be selected via software, according to the specific setup and acquisition mode.

Common trigger: all channels acquire simultaneously with a common trigger. The trigger can be fed externally or generated by a combination of individual channel discriminators. This mode is mainly intended for the acquisition of waveforms, like a digital oscilloscope. Options for zero suppression are available to remove not significant data

Independent trigger: suited for trigger-less applications, where no global trigger is needed but each channel acquires waveforms upon its self-trigger which fires through a digital discriminator, independently of the others.

DPP: real-time processing in the FPGA allows for the extraction of physical parameters from the waveform (e.g. pulse height, charge, timestamp, PSD), well suited for high counting rate applications. It is yet possible to save both raw waves and parameters.




## FPGA

A template of the firmware is available for customers who want to personalize the acquisition to implement custom algorithms for pulse processing in the open FPGA. The user can have control of the data output information and customize the trigger logic to get several combinations of self-triggers and I/O signals to validate or discard the events. Custom software can run on the onboard CPU for data reduction and analysis..

## Synchronization

Multi-board synchronization can be implemented via backplane or front panel easy-cabling options.

## Connectivity

Multi-interface: USB-3.0 and CONET* optical link or 1/10 Gb Ethernet (switchable on the same socket)

(*) *CONET: CAEN Daisy Chainable Optical Link Protocol*

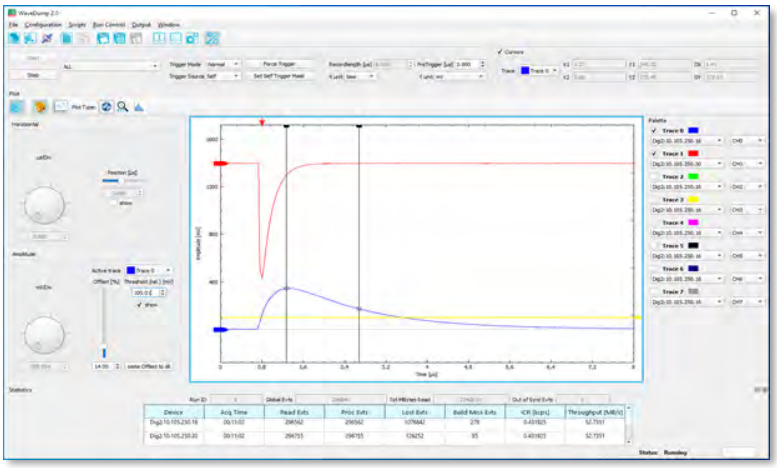

## Data Acquisition

The 2740/2745 Digitizer can manage the entire acquisition chain, from the input signal sampling in the ADC to the processing of the signal and readout. Thanks to the open FPGA, it is possible to customize the firmware for pulse processing, while the Arm hosted onboard permits writing custom software. These features allow obtaining a highly compact and flexible readout module that can be tailored to different types of applications: nuclear spectroscopy with segmented germanium detectors, readout of Silicon strips, waveform capture for gamma-ray tracking, sub-ns timing measurements are among the possibilities.

For those users who do not need to customize the digital pulse processing, we provide a series of firmware and software for:

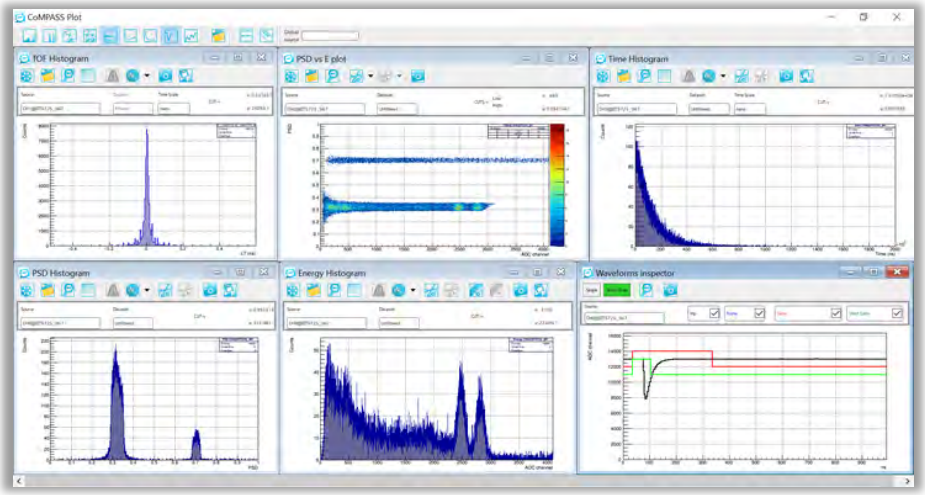
- Waveform recording using common-trigger
- Energy Spectrum recording using PHA (QDC, PSD, etc.) mode
- Pulse shape discrimination
- Sub-ns timing measurements using digital CFD
- Advanced Waveform readout using ZLE (Zero Length Encoding) or DAW (Dynamic Acquisition Window)

CAEN provides two ready-to-use user-friendly readout software: WaveDump2 for waveform recording using common-trigger firmware and CoMPASS, a multiparametric DAQ software to manage the other Digital Pulse Processing algorithms. Multiple boards can even be managed providing a simultaneous plot of waveforms and other quantities of interest.



### WaveDump2 software

- Multi-board management
- Simultaneous plot of waveforms from up to 8 input channels
- Flexible and easy configuration of channel and trigger settings
- FFT analysis



### CoMPASS multiparametric software

- Simultaneous plot of waveforms, Time, Energy, PSD, and TOF spectra
- Online filtering (Time, Energy, PSD)
- Multi-board management
- Advanced data saving

# Technical Specifications

## General Features

| Analog Inputs | | |
|---|---|---|
| Number of Channels | 64 | Differential on 274x version / Single-ended on 274xB version |
| Impedance | 50 Ω (Single-ended) | 100 Ω (Differential) |
| Connector | Four 2mm 40-pin header male Input adapters available | |
| | **2740** | **2745** |
| Full scale range (FSR) | 2 $V_{pp}$ | 4 $V_{pp}$ |
| Individual Offset adjustable in the range | ±1.25V | ± 2.5V |
| Bandwidth (-3 dB) | 50 MHz | 20 MHz |
| Gain | x1 | x1 to x100 In steps of 0.5 dB |
| **Digital Conversion / System Performance** | | |
| Resolution | 16 bits | |
| Sampling Rate | 125 MS/s (simultaneously on each input) | |
| | **2740** | **2745** |
| ENOB | 11.7 (Typ.) | 12.0 (Typ. @5 MHz, -3dB, Gain x1) |
| RMS | 3.9 LSB (~ 120 µV) typical | 3.6 LSB RMS (@Gain x1) |

| Digital I/O and Analog Output | | |
|---|---|---|
| CLK-IN | Two differential pairs:<br>- CLK: reference clock signal<br>- SYNC: synchronization signal (start/stop, T0, etc.) | AC-coupled LVDS, ECL, PECL, LVPECL, CML<br>Zdiff = 100 Ω<br>2.54mm 4-pin AMPMODU Mod II male connector |
| CLK-OUT | Same functionalities as CLK-IN<br>Daisy chainable in multi-board synchronization | LVDS<br>2.54mm 4-pin AMPMODU Mod II male connector |
| TRG-IN/TRG-OUT/GPIO/S-IN | General-purpose I/Os<br>Software programmable (trigger, gate, veto, busy, etc.)<br>- TRG-IN/S-IN internally terminated with 50 Ω (Zin = 50 Ω)<br>- TRG-OUT requires Rt = 50 Ω<br>- GPIO as Input must be terminated with 50 Ω<br>- GPIO as TTL Output requires Rt = 50 Ω<br>- GPIO as NIM Output requires Rt = 50 Ω or 25 Ω | Sigle-ended TTL/NIM<br>LEMO 00 male connector |
| LVDS I/O | 16 differential pairs<br>Software programmable I/O (individual self-trigger outputs, trigger validations, Veto, Busy, Start, Stop, Pattern Input, etc.) | LVDS<br>Zdiff = 100 Ω (when set as inputs)<br>2.54mm 34-pin AMPMODU Mod II male connector |
| DAC OUT | DAC output for signal inspection, pulse generation, majority level<br>14-bit Digital-to-Analog Converter (DAC)<br>125 MS/s Update Rate | ±1 V @ 50Ω load<br>±2 V @ hi-Z load Output Range<br>LEMO 00 connector |

# Technical Specifications (continued)

## Acquisition Memory

| | |
|---|---|
| | 2.5 GB total DDR4 memory size (20.971 MS/ch) divisible in multiple buffers<br>Maximum record length: ~ 168 ms @ 125 MS/s (total memory size divided by 2)[1]<br>[1] *Value referred to the Scope firmware (minimum of two buffers admitted)* |

## Communication Interfaces

| | | |
|---|---|---|
| 1/10 Gigabit Ethernet | SFP+ receptacle for 1/10 GbE Copper (RJ-45) or Optical links (50/125µm OM2 or OM3 fiber)<br>TCP-IP stack implemented in the on-board Arm<br>Transfer rate sustained: 110 MB/s @1Gb | |
| USB | USB-3.0 version<br>Transfer rate sustained: 280 MB/s | Type-C Connector |
| Optical Link (optional) | CONET, CAEN proprietary protocol | |

## Trigger and Synchronization

| | | |
|---|---|---|
| **Trigger Modes** | | |
| Common | All channels acquire simultaneously with the trigger (software, external or logic combination of self-triggers) | |
| Individual | Each channel acquires independently with its self-trigger | |
| Correlated | The individual self-trigger of each channel is validated by the coincidence/anticoincidence logic between other self-triggers and/or external I/Os | |
| **Synchronization** | | |
| Clock Propagation | Typical 62.5MHz frequency distributed by daisy chain through CLK-IN/CLK-OUT or by fan-out to CLK-IN<br>Custom frequencies can be supported | |
| Acquisition Start/Stop | Daisy chain or fan-out propagation through CLK-IN/CLK-OUT or NIM/TTL, LVDS I/O | |
| Data Sync | Busy/Veto logic on LVDS I/Os or NIM/TTL I/Os for event building synchronization | |
| Trigger Time Stamp | Zero from START or S-IN input<br>Resolution: 8 ns | Counter range: 48 bits<br>Full-scale range: ~625 h |
| Trigger Distribution | TRG-IN/TRG-OUT NIM/TTL LEMO I/Os (common trigger) or LVDS I/Os (common or individual trigger) | |

## Firmware and FPGA

| | | |
|---|---|---|
| **Firmware** | **Firmware stored in the on-board Flash Memory and live rebootable by Web Interface** | |
| DPP Firmware | DPP Firmware Implements the digital pulse processing algorithm:<br>- DPP-PHA: Pulse Height Analysis<br>- DPP-QDC: Charge Integration<br>- DPP-PSD: Pulse Shape Discrimination | - DPP-ZLE: Zero Length Encoding<br>- DPP-DAW: Dynamic Acquisition Window |
| Scope Firmware | Firmware for the waveform recording | |
| Upgrades | Any supported firmware can be uploaded via Web Interface (both different firmware types and upgraded versions of the same firmware) | |
| **FPGA** | | |
| Device | Xilinx Zynq UltraScale+ Multiprocessor System-on-Chip mod. XCZU19EG<br>Processing System based on Quad-core Arm with 2GB DDR4 memory @2400 MT/s (Linux OS onboard)<br>Programmable logic with more than 1100K system logic cells and 80Mbit memory | |
| **Open FPGA** | | |
| User-Scope Template | Common trigger, simultaneous waveform recording on 64 channels management. Trigger logic and wave processing customization | |
| User-DPP Template | Individual trigger and channel acquisition management. Customization of DPP algorithm, trigger logic, and event data information | |

# Technical Specifications (continued)

## Software

| Readout Software |
|---|
| CoMPASS spectroscopy software (for DPP firmware only) |
| WaveDump2 (for Scope firmware only) |
| **Web Interface** |
| Firmware management (e,g. upgrades and on-the-fly selection of the firmware to run), board information, PLL and Ethernet configuration, board status monitoring |
| **SDK and Tools** |
| General-purpose C libraries with demo samples for host Windows® and Linux® PC, and embedded Arm processor |

## Mechanical

| | V2740 / V2740B | VX2740 / VX2740B | DT2740 / DT2740B / DT2745 / DT2745B | |
|---|---|---|---|---|
| Form Factor | 1-unit wide VME64 | 1-unit wide VME64X 6U | Desktop | Desktop-Rack |
| Weight | 642 g | 642 g | 3120 g | 3170 g |
| Dimension | | | 337 W x 96 H x 278 L mm³ (without connectors) | 19" rack mount |

## Environmental

| | |
|---|---|
| Environmental | Indoor use |
| Operating Temperature | 0°C ÷ +40°C |
| Storage Temperature | -10°C ÷ +60°C |
| Operating Humidity | 10% ÷ 90% RH non condensing |
| Storage Humidity | 5% ÷ 90% RH non condensing |
| Pollution Degree | 2 |
| Altitude | ≤2000 m |
| Overvoltage Category | II |
| EMC Environment | Commercial and light industrial |
| IP Degree | Enclosure (desktop models), not for wet location |

## Regulatory

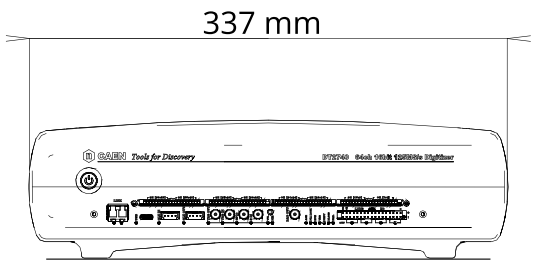
| | |
|---|---|
| Compliance | EMC: CE 2014/30/EU Electromagnetic compatibility Directive<br>Safety: CE 2014/35/EU Low Voltage Directive |

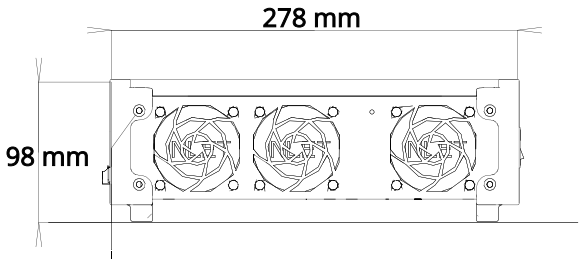
## Power Requirements

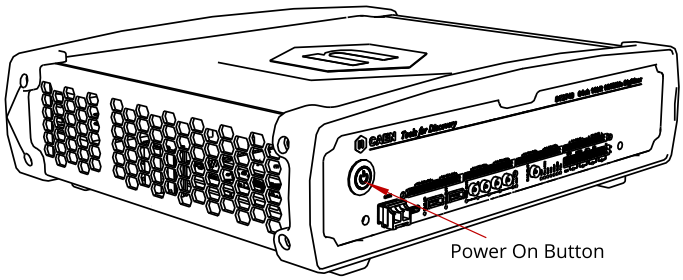
| | V2740 / V2740B | VX2740 / VX2740B | DT2740 / DT2740B |
|---|---|---|---|
| + 12V | 0.9 A (Typ) | 0.9 A (Typ) | - |
| + 5 V | 6.7 A (Typ) | 3.6 A (Typ) | - |
| + 3.3 V | - | 4.4 A (Typ) | - |
| | | | Mains Powered (Max. 130 Watt @ 110/220V) |

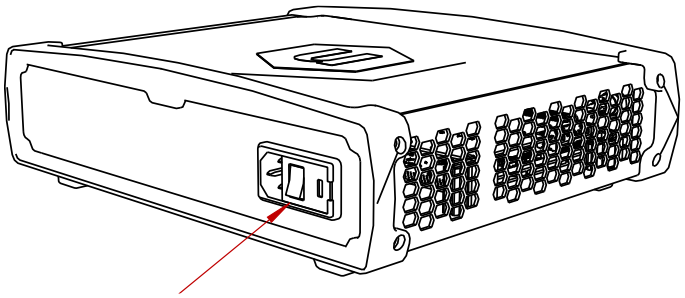
| | V2745 / V2745B | VX2745 / VX2745B | DT2745 / DT2745B |
|---|---|---|---|
| + 12V | t.b.d. | 1.4 A (Typ) | - |
| + 5 V | t.b.d. | 5.4 A (Typ) | - |
| + 3.3 V | - | 4.8 A (Typ) | - |
| | | | Mains Powered (Max. 130 Watt @ 110/220V) |

## DT2740/DT2745 Mechanical Dimension

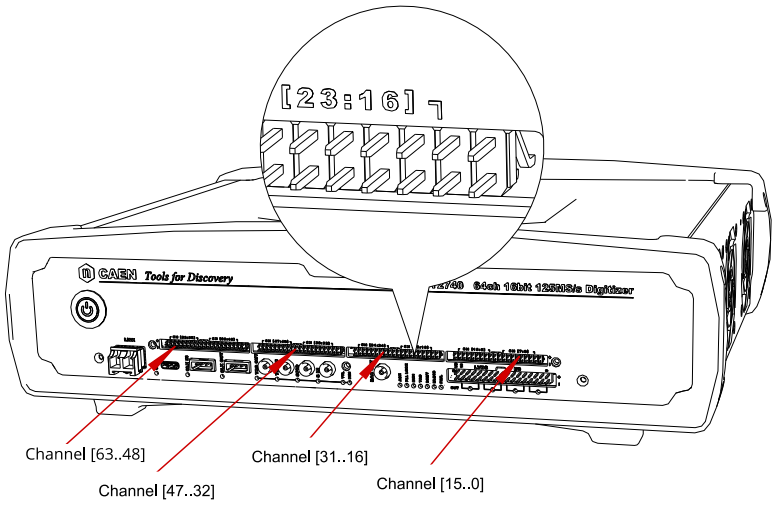


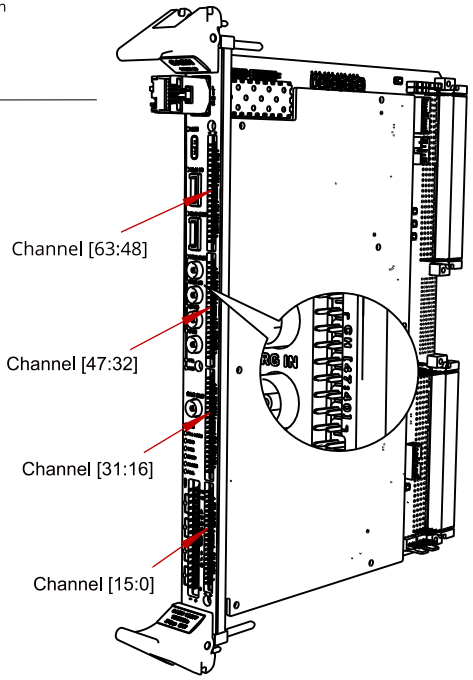



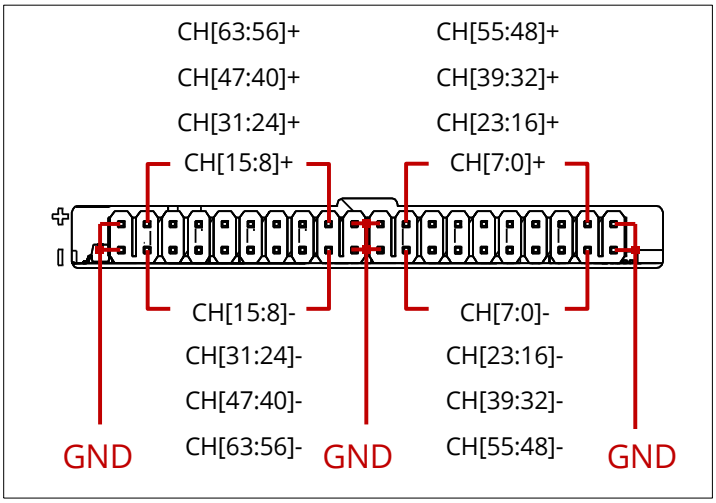




## 2740/2745 Analog Input Pinout

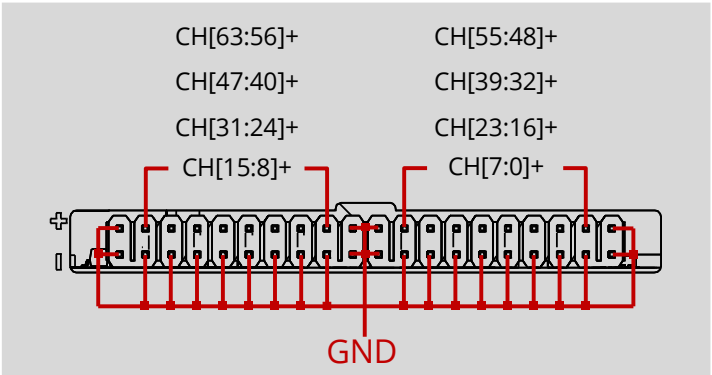


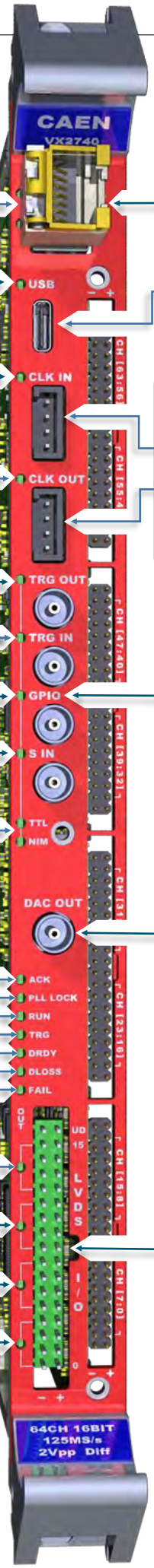

### Differential (2740/2745)




### Single-ended (2740B/2745B)



## 2740/2745 Front Panel and LED behavior




**LINK** Ethernet network indicator
- Ethernet link unavailable (cable off)
- Ethernet link available (cable in)
- Data activity on the ethernet link

**USB** USB Link Indicator
- USB link unavailable (cable off)
- USB link available (cable in)
- Data activity on the USB link

**CLK IN** Reference Clock indicator
- Internal clock reference enabled
- External clock reference enabled

**CLK OUT** Reference Clock indicator
- Reference clock propagation disabled
- Reference clock propagation enabled

**TRG OUT**
**TRG IN**
**GPIO**
**S IN**
LEMO I/O level indicator
- No activity on the relevant connector
- Signal activity on the relevant connector

**TTL / NIM** LEMO I/O level indicator
- NIM or TTL level enabled for the 4 LEMO I/Os

**ACK** Readout activity indicator
- No readout access to the board through USB or Ethernet
- Read or Write access to the board through USB or Ethernet

**PLL LOCK** PLL lock indicator
- The PLL is not locked to the reference clock
- The PLL is locked to the reference clock

**RUN** Acquisition (data taking) indicator
- The acquisition is off
- The acquisition is running

**TRG** Accepted Trigger indicator
- The trigger is accepted

**DRDY** Data ready indicator
- Event/Data is present in the Output Buffer

**DLOST** Data loss indicator
- The trigger arrived while the board is in busy state. This trigger is rejected and the relevant event/data is lost

**FAIL** Board fail indicator
- A power fail, over temperature condition or PLL lock loss occurred

**OUT** LVDS I/O direction indicator
- LVDS I/O 4-pin group direction is INPUT
- LVDS I/O 4-pin group direction is OUTPUT

**LINK** Ethernet Transceiver (inserted in the SFP+ receptacle)

**USB** Type-C Connector

**CLK-IN / CLK-OUT** 2.54mm 4-pin AMPMODU Mod II male connector

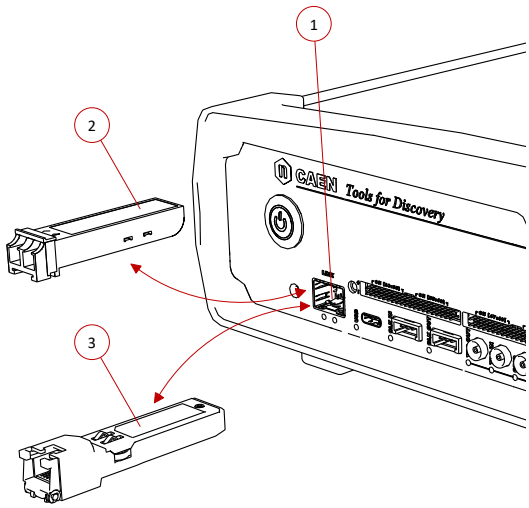

General Purpose I/O
**TRG-IN / TRG-OUT / GPIO / S-IN**
LEMO 00 connector

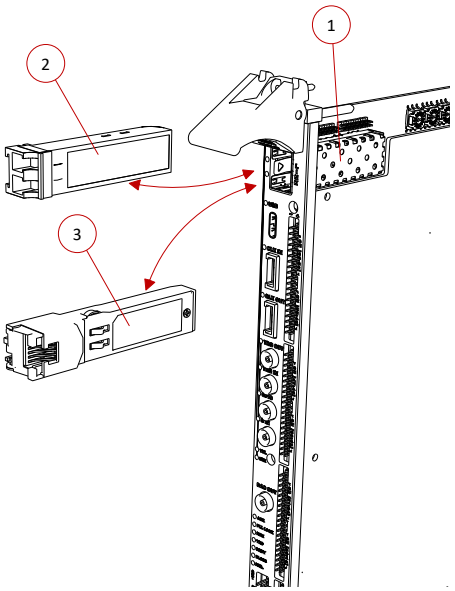
**DAC-OUT** LEMO 00 connector

**LVDS I/O** 16 differential pairs

**LED mode**
- OFF
- ON (COLOR)
- BLINKING (COLOR)

## 2740/2745 SFP+ receptacle for 1/10 GbE Copper (RJ-45) or Optical links




1. SFP+ receptacle for 1/10 GbE Copper (RJ-45) or Optical links
2. Optical Transceiver
   Type: AFBR-710DMZ Manufacturer: Avago
3. Ethernet Transceiver
   Cisco Compatible 1000Base-T Copper SFP (mini-GBIC) Transceiver

## 2740/2745 Accessories

### A372F

#### 64 channel 2.54mm Male Header Connector Adapter

The A372F adapter is compliant to all the form factors of the 2740 digitizer. It mecanically adapts to 2.54mm header from the 2mm header mounted on the digitizer, independently of the differential or single-ended standard of the 2740 analog channels.

Dedicated metal supports fixed by screws give stress resistance when plugged in the digitizer inputs.

### A319A

#### Clock & Sync cable assembly

The A319A is a cable assembly for the Clock and Sync signal distribution in 2740 Digitizer Through the front panel CLK-OUT / CLK-IN daisy chain, this 4-contact cable carries two differential signals from one digitizer to another to synchronize multiple boards.

### A372M

#### 64 channel MCX Coax Connector Adapter for SE signals

The A372M applies to the 64-channel 2740 Digitizer Family. It must be used with the single-ended input 2740 models and adapts to MCX Coaxial from the 2mm header mounted on the digitizer.

Metal supports fixed by screws give stress resistance when the adapter is mounted in the 2740 digitizer inputs.

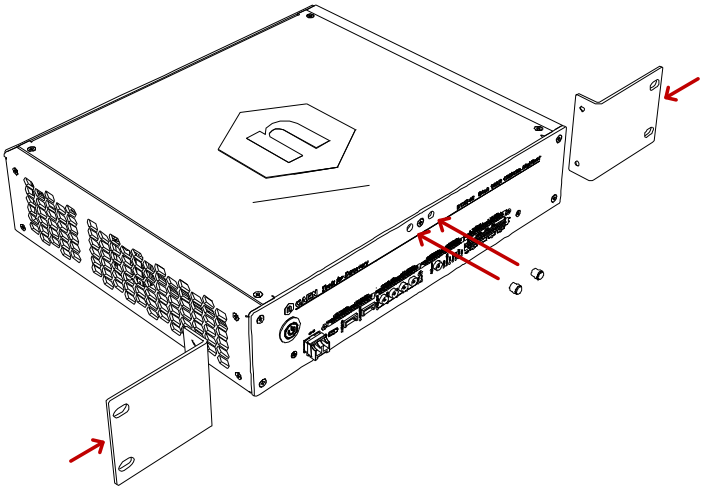
### A319B

#### Clock cable assembly from 2740 series to Standard Digitizers

The A319B is a cable assembly for the Clock signal distribution between non homogenous digitizer series, matching the 3-contact connector on the Standard Digitizer to the 4 -pin connector on the 2740 Digitizer Series. Through the front panel CLK-OUT / CLK-IN daisy chain, this cable carries the differential clock signal from one digitizer to another to synchronize multiple boards .

## Rack Mounting:

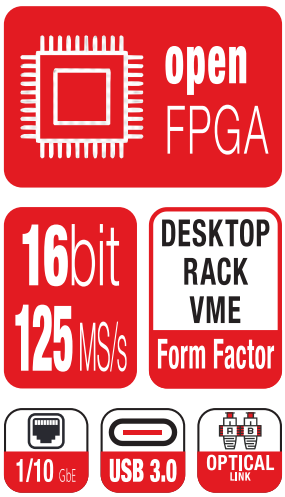
Desktop digitizers (DT5740x/DT5745x) can be rack mounted using 2 brackets included in the product-kit.




## Ordering Option

| Description | Code |
|---|---|
| V2740 - 64 Ch 16 bit 125MS/s Digitizer, Diff | WV2740XAAAAA |
| V2740B - 64 Ch. 16 bit 125 MS/s Digitizer, SE | WV2740BXAAAA |
| VX2740 - 64 Ch 16 bit 125MS/s Digitizer, Diff | WVX2740XAAAA |
| VX2740B - 64 Ch. 16 bit 125 MS/s Digitizer, SE | WVX2740BXAAA |
| DT2740 - 64 Ch 16 bit 125MS/s Digitizer, Diff | WDT2740XAAAA |
| DT2740B - 64 Ch. 16 bit 125 MS/s Digitizer, SE | WDT2740BXAAA |
| V2745 - 64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, Diff | WV2745XAAAAA |
| V2745B - 64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, SE | WV2745BXAAAA |
| VX2745 - 64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, Diff | WVX2745XAAAA |
| VX2745B - 64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, SE | WVX2745BXAAA |
| DT2745 - 64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, Diff | WDT2745XAAAA |
| DT2745B - 64 Ch. 16 bit 125 MS/s Digitize with Programmable Input Gain, SE | WDT2745BXAAA |
| ***Accessories*** | |
| A372F - 64 channel Adapter to 2.54mm Male Header Connector for Digitizer Series 2.0 | WA372FXAAAAA |
| A372M - 64 channel Adapter to MCX Coax Connector for Digitizer Series 2.0 | WA372MXAAAAA |
| A319A - Clock & Sync Cable for Digitizers Series 2.0 interconnection (L=20cm) | WA372MXAAAAA |
| A319B - Clock Cable for Digitizer Series 1.0 to 2.0 interconnection (L=20cm) | WA319BXAAAAA |

2740/2745
Digitizer Family

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